1. Table 1 shows SPEC2000 performance for SPEC CFP2000. The reference time is the execution time for a particular computer system chosen by SPEC as a performance reference for all other tested systems. The base ratio is simply the run time for a benchmark divided into the reference time and is expressed as a percentage. The SPECfp_based2000 statistic is computed as the geometric mean of the base ratios.
   (1) Calculate the SPECfp_based2000 statistic and fill in Table 1. (5%)
   (2) Calculate the weights for a workload so that running times on the reference computer will be equal for each of the three programs in Table 1. (5%)
   (3) Using the weights computed in part (2), calculate the weighted arithmetic means of the execution times of the three programs in Table 1. (6%)

2. Consider adding a new index addressing mode to MIPS. The addressing mode adds two registers and an 11-bit signed offset to get the effective address. Our compiler will be changed so that code sequences of the form

   ADD   R1, R1, R2
   LW   Rd, 100(R1)   (or store)

   will be replaced with a load (or store) using the new addressing mode. If loads and stores comprise 26% and 10% of the average instruction mix respectively, use the average instruction frequencies in evaluating this addition.
   (1) Assume that the addressing mode can be used for 10% of the displacement loads and stores (accounting for both the frequency of this type of address calculation and the shorter offset). What is the ratio of instruction count on the enhanced MIPS compared to the original MIPS? (9%)
   (2) If the new addressing mode lengthens the clock cycle by 5%, which machine will be faster and by how much? (9%)

3. In Table 2, show what the information tables of Tomasulo's algorithm look like when only the first load has completed and written its result. (12%)

4. A branch-target buffer offers potential performance gains, but at a cost. Power consumption and clock cycle time may be critical design issues for a processor. Discuss the effect that a branch-target buffer has on these parameters as a function of buffer size. How is this BTB effect on power and clock cycle time similar to or different from that of other pipeline structures, such as the register file or ALU? What ways can you think of to improve the benefits of a BTB while at the same time meeting or exceeding power consumption and clock cycle time goals? (10%)

5. As caches increase in size, blocks often increase in size as well.
   (1) If a large instruction cache has larger data blocks, is there still a need for prefetching? Explain the interaction between prefetching and increased block size in instruction caches. (6%)
   (2) Is there a need for data prefetch instructions when data blocks get larger? Explain. (6%)

6. Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. What are the various miss rates? Assume the miss penalty from the L2 cache to memory is 100 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle, and there are 1.5 memory references per instruction. What is the average memory access time and average stall cycles per instruction? Ignore the impact of writes. (16%)

7. Answer the following questions.
   (1) Please explain the usefulness and limitation of the conditional (or predicated) instructions. (5%)
   (2) Use the optimization technique of tree height reduction to increase the parallelism of the following code. (5%)

   ADD   R3, R1, R2
   ADD   R5, R3, R4
   ADD   R7, R5, R6
   ADD   R9, R7, R8
   ADD   R11, R9, R10

   (3) Please briefly explain the techniques to improve the bandwidth of DRAM: Fast Page Mode, SDRAM, and DDR. (6%)

Table 1

SPEC CFP2000 program name	Reference time	Base ratio		Equal-time weightings	Weighted time for each benchmark (seconds)		
		Machine A	Machine B		Reference computer	Machine A	Machine B
Program 1	160	460	300				
Program 2	310	1080	230				
Program 3	220	400	260				
SPECfp_based2000							
Weighted arithmetic mean							

Table 2

Instruction	Issue	Execute	Write Result
L.D F6, 34(R2)	√	√	√
L.D F2, 45(R3)	√	√	
MUL.D F0, F2, F4	√		
SUB.D F8, F2, F6	√		
DIV.D F10, F0, F6	√		
ADD.D F6, F8, F2	√		

Name	Busy	Op	Vj	Vk	Qj	Qk	A
Load1	no						
Load2	yes						
Add1	yes						
Add2	yes						
Add3	no						
Mult1	yes						
Mult2	yes						

Field	F0	F2	F4	F6	F8	F10	F12	...	F30
Qi	Mult1								