國立中山大學資訊工程學系

94 學年度第 2 學期博士班資格考試　計算機結構

1. To keep the issue step of the statically scheduled superscalar MIPS processor quite simple, an issue limit of one integer and one floating-point instruction per clock was imposed. Let's remove this restriction and see how issue step workload grows with increasing multiple-issue capability. Assume a five-stage superscalar pipeline (IF, ID, EX, MEM, WB) with no issue restrictions and no structural hazards. Also, regardless of instruction, each stage always takes just 1 clock cycle to complete its task, and an instruction may have up to two operands and one result. Assuming that the register file forwards values that are read and written during the same clock cycle.
   (1) The ID stage must check for what type(s) of data dependences? (6%)
   (2) For a two-issue design with 128 integer registers and 128 floating-point registers, how many bits must be brought to comparators in the ID stage and how many comparisons must be performed during each clock cycle to check just for data hazards? (6%)
   (3) Let the issue limit be *n* instructions, and assume the total number of registers is unbounded. How many comparisons, as a function of *n*, must be performed to check just for data hazards? (6%)

2. Consider the following MIPS assembly code.

```
LD      R1, 45(R2)
DADD    R4, R3, R5
DSUB    R2, R1, R4
OR      R4, R6, R3
BNEZ    R7, target
DADD    R7, R5, R8
```

   (1) Identify each dependence by type; list the two instructions involved; identify which instruction is dependent; and, if there is one, name the storage location involved. (8%)
   (2) For each pair of instructions with dependences that you found in part (1), discuss whether dynamic scheduling is, may be, or is not sufficient to allow out-of-order execution of these instruction pairs. (8%)

3. Suppose we have a deeply pipelined processor, for which we implement a branch-target buffer for the conditional branches only. Assume that the misprediction penalty is always 4 cycles and the buffer miss penalty is always 3 cycles. Assume 80% hit rate and 90% accuracy, and 20% branch frequency. How much faster is the processor with the branch-target buffer versus a processor that has a fixed 2-cycle branch penalty? Assume a base CPI without branch stalls of 1.5. (15%)

4. Consider the following code fragment from an if-then-else statement of the form

If (A==0) A = B; **else** A = A+4;

where A is at 0(R3) and B is at 0(R2):

```
LD      R1,0(R3)          ; load A
        BNEZ    R1,L1     ; test A
        LD      R1,0(R2)  ; then clause
        J       L2        ; skip else
L1 :    DADDI   R1,R1,#4  ; else clause
L2 :    SD      R1,0(R3)  ; store A
```

Assume R14 is unused and available.

(1) Assume the then clause is almost always executed. Compile the code using compiler-based speculation. (5%)

(2) Show how the example can be coded using a speculative load (sLD) and a speculation check instruction (SPECCK) to completely preserve exception behavior. (5%)

(3) Show how it would be compiled with speculative instructions and poison bits. Show where an exception for the speculative memory reference would be recognized. (5%)

5. Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. What are the various miss rate? Assume the miss penalty from the L2 cache to memory is 100 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle, and there are 1.5 memory references per instruction. What is the average memory access time and average stall cycles per instruction? Ignore the impact of writes. (12%)

6. Answer the following questions.

(1) Please describe the features of the instruction set architectures for media and signal processing applications from the point of view of addressing modes, type and size of operands, and operations. (6%)

(2) The major complication in implementing predicated instructions is deciding when to annul an instruction. Please explain the advantages and disadvantages when predicated instructions are annulled early or later in the pipeline. (6%)

(3) You can apply the *wider main memory* or *simple interleaved memory* to obtain higher memory bandwidth. Please explain and compare the two techniques. (6%)

(4) Please explain what the translation lookaside buffer (TLB) is and why it is necessary. (6%)