國立中山大學資訊工程學系

100 學年度第 1 學期博士班資格考試　計算機結構

1. Early examples of CISC and RISC design are the VAX 11/780 and the IBM RS/6000, respectively. Using a typical benchmark program, the following machine characteristics result:

Processor	**Clock Frequency**	**Performance**	**CPU Time**
VAX 11/780	5 MHz	1 MIPS	12 *x* seconds
IBM RS/6000	25 MHz	18 MIPS	*x* seconds

The final column shows that the VAX required 12 times longer than the IBM measured in CPU time.

(1) (4%) What is the relative size of the instruction count of the machine code for this benchmark program running on the two machines?

(2) (6%) What are the CPI (cycles per instruction) values for the two machines?

2. Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size.

(1) (6%) Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

(2) (6%) Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

(3) (8%) Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag.

3. Consider a paged logical address space (composed of 32 pages of 2 KBytes each) mapped into a 1-MByte physical memory space.

(1) (4%) What is the format of the processor's logical address?

(2) (4%) What is the length and width of the page table (disregarding the "access rights" bits)?

(3) (4%) What is the effect on the page table if the physical memory space is reduced by half?

4. A nonpipelined processor has a clock rate of 2.5 GHz and an average CPI of 4. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays, such as latch delay, the clock rate of the new processor has to be reduced to 2 GHz.

(1) (6%) What is the speedup achieved for a typical program?

(2) (6%) What is the MIPS rate for each processor?

5. Figure 1 shows an example of a superscalar processor organization. The processor can issue two instructions per cycle if there is no resource conflict and no data dependence problem. There are essentially two pipelines, with four processing stages (fetch, decode, execute, and store). Each pipeline has its own fetch decode and store unit. Four functional units (multiplier, adder, logic unit, and load unit) are available for use in the execute stage and are shared by the two pipelines

on a dynamic basis. The two store units can be dynamically used by the two pipelines, depending on availability at a particular cycle. There is a lookahead window with its own fetch and decoding logic. This window is used for instruction lookahead for out-of-order instruction issue. Consider the following program to be executed on this processor:

```
I1:  Load R1, A        /R1 ← Memory (A)/
I2:  Add R2, R1        /R2 ← (R2) + R(1)/
I3:  Add R3, R4        /R3 ← (R3) + R(4)/
I4:  Mul R4, R5        /R4 ← (R4) + R(5)/
I5:  Comp R6           /R6 ← (R6)/
I6:  Mul R6, R7        /R3 ← (R3) + R(4)/
```

(1) (6%) What dependencies exist in the program?

(2) (6%) Show the pipeline activity for this program on the processor of Figure 1 using in-order issue with in-order completion policies and using a presentation similar to Figure 2.

(3) (6%) Repeat for in-order issue with out-of-order completion.

(4) (6%) Repeat for out-of-order issue with out-of-order completion.

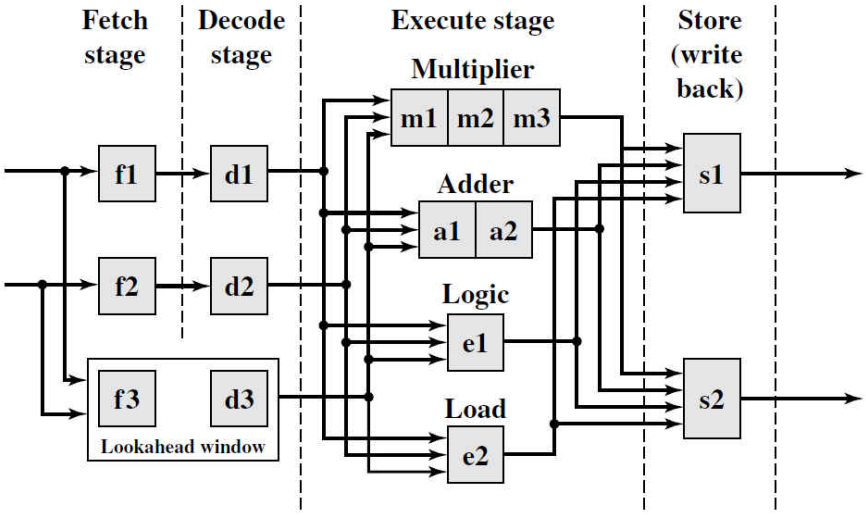

Figure 1

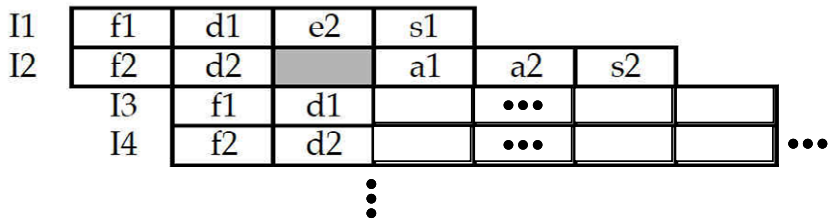

Figure 2

6. Please answer the following questions.

(1) (6%) Briefly explain the following three techniques for I/O operations: programmed I/O, interrupt-driven I/O, and direct memory access.

(2) (6%) List and briefly explain three ways in which an instruction pipeline can deal with conditional branch instructions.

(3) (4%) What is the difference between the superscalar and superpipelined approaches?

(4) (6%) What are interleaved multithreading, blocked multithreading, and simultaneous multithreading (SMT)?