國立中山大學資訊工程學系

99 學年度第 1 學期博士班資格考試　計算機結構

1. (8%)　A common transformation required in graphics processors is square root. Implementations of floating-point (FP) square root vary significantly in performance, especially among processors designed for graphics. Suppose FP square root (FPSQR) is responsible for 30% of the execution time of a critical graphics benchmark. One proposal is to enhance the FPSQR hardware and speed up this operation by a factor of 10. The other alterative is just to try to make all FP instructions in the graphics processor run faster by a factor of 2; FP instructions are responsible for half of the execution time for the application. The design team believes that they can make all FP instructions run 2 times faster with the same effort as required for the fast square root. Compare these two design alternatives.

2. (8%)　Suppose we have made the following measurements:
   - Frequency of FP operations = 25%
   - Average CPI (clocks per instruction) of FP operations = 4.0
   - Average CPI of other instructions = 1.33
   - Frequency of FPSQR = 2%
   - CPI of FPSQR = 20

   Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operation to 2.5. Compare these two design alternatives using the processor performance equation.

3. (1) (6%)　Explain what dynamic scheduling is and describe its advantages and disadvantages when compared to static scheduling.

   (2) (4%)　Explain the purpose of register renaming.

   (3) (12%)　Show what the information tables (Table 1) of Tomasulo's algorithm look like when only the first load has completed and written its result.

4. (1) (7%)　Please describe two alternative architectural approaches and associated communication mechanisms for communicating data among processors in the large-scale multiprocessor.

   (2) (12%)　Suppose we have an application running on a 32-processor multiprocessor, which has a 200 ns time to handle reference to a remote memory. For this application, assume that all the references except those involving communication hit in the local memory hierarchy, which is slightly optimistic. Processors are stalled on a remote request, and the processor clock rate is 2 GHz. If the base CPI (assuming that all references hit in the cache) is 0.5, how much faster is the multiprocessor if there is no communication versus if 0.3% of the instructions involve a remote communication reference?

5. (1) (10%) There are three metrics for cache optimizations: hit time, miss rate, and miss penalty. Please explain the following techniques and the metrics that they can reduce: way prediction and compiler optimizations.

(2) (8%) Assume we have a computer where the CPI is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 30 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits?

(3) (10%) Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. What are the various miss rates? Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle, and there are 1.5 memory references per instruction. What is the average memory access time and average stall cycles per instruction? Ignore the impact of writes.

6. Please answer the following questions.

(1) (5%) Explain what loop unrolling is and describe its advantages and disadvantages.

(2) (5%) Explain the differences between branch prediction buffers and branch target buffers.

(3) (5%) Explain the differences between instruction-level parallelism and thread-level parallelism.

Table 1

		Instruction status		
Instruction		**Issue**	**Execute**	**Write Result**
L.D	F6, 32(R2)	√	√	√
L.D	F2, 44(R3)	√	√	
MUL.D	F0, F2, F4	√		
SUB.D	F8, F2, F6	√		
DIV.D	F10, F0, F6	√		
ADD.D	F6, F8, F2	√		

	Reservation stations						
Name	**Busy**	**Op**	**Vj**	**Vk**	**Qj**	**Qk**	**A**
Load1	no						
Load2	yes	Load					
Add1	yes	SUB					
Add2	yes	ADD					
Add3	no						
Mult1	yes	MUL					
Mult2	yes	DIV					

Register status									
Field	**F0**	**F2**	**F4**	**F6**	**F8**	**F10**	**F12**	• • •	**F30**
Qi	Mult1								