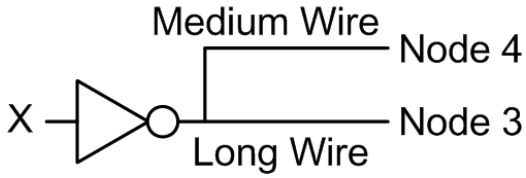
Dept. of Computer Science and Engineering, National Sun Yat-sen Univ.
Second Semester of 2019 PhD Qualifying Exam

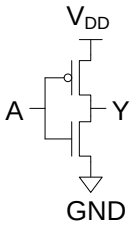
Subject：Electronics

1. (10%) The following figure models a gate driving wires to two destinations. The gate is represented as a voltage source with effective resistance *R*. The two receivers are located at nodes 3 and 4. The wire to node 3 is long enough that it is represented with a pair of π-segments, while the wire to node 4 is represented with a single segment. We assume the parasitic capacitances in this circuits all are equal to *C* and the wire resistance in a single π-segment is *R*.



   a. (5%) Please draw the effective RC circuit.
   b. (5%) Please find the Elmore delay from input *x* to each receiver.

2. (65%) In the following problems, assume that the length of all MOS transistors are 1um. In a particular process technology, a CMOS inverter with pMOS width W_p=2um and nMOS width W_n=1um has equal propagation fall delay and rise delay $T_{pHL} = T_{pLH} = T_{inv}$ of output switching from high to low and output switching from low to high respectively. The following Figure shows the circuit and the corresponding SPICE netlist.

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VDD vdd gnd 1.8v
M1 y a gnd gnd NMOS W=1U L=1U
M2 y a vdd vdd PMOS W=2U L=1U
Vin a gnd pulse 0 1.8v 25ps 0ps 0 ps 35ps 80ps
* pulse v1   v2   td   tr   tf   pw   per
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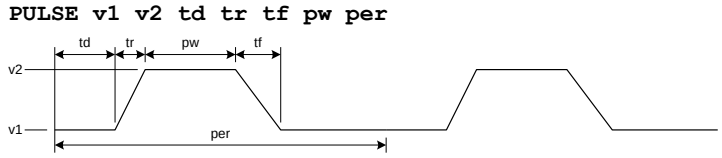


2.1. (5%) Draw the static CMOS circuit diagram of a three-input NAND gate (named NAND3) whose Boolean function is $Y = \overline{ABC}$. Hint: CMSO NAND3 consists of a pull-up pMOS network with three pMOS transistors and a pull-down nMOS network with three nMOS transistors.

2.2. (15%) Write down the SPICE netlist that describes the CMOS NAND3 circuits. Hint: the SPICE list contains 6 SPICE statements starting with M… indicating MOS transistors, and 1 statement starting with V… indicating the power supply.

2.3. (10%) Draw the waveforms of the three inputs so that they can be used to measure the "worse-case" propagation delay from the input A to the output Y. Hint: worse-case delay happens when only one MOS is ON in case of MOS transistors connected in parallel.

2.4. (5%) Write down the SPICE netlist that generates the above input waveforms. Hint: the SPICE list contains 3 SPICE statements staring with V

2.5. (5%) Design the static CMOS circuit for three-input AND gate (named AND3) $Y = ABC$. How many transistors are required? Note that in static CMOS design, the output should be either strong (good) logic "1" or strong (good) logic "0). How many transistors are required?

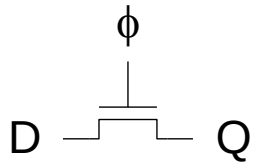
2.6. (5%) Design a circuit for AND3 with fewer transistors than static CMOS AND3. Compare it with the static CMOS AND3 in the previous problem. Hint: AND3 circuit with weak logic "1" or logic "0" might have fewer transistors.

2.7. (10%) A two-to-one multiplexer (named MUX2) can be represented by Boolean function $SD_0 + \bar{S}D_1$. Use CMOS NAND2, NOR2, and inverters to construct MUX2. How many transistors are required in this circuit?

2.8. (10%) Draw the circuit diagram for following circuit layout with inputs A, B, and output Y. What is the logic function of the layout?

3. (25%) Answer the following questions about

3.1. (10%) The simplest D-latch circuit design is a single nMOS shown below. It has many drawbacks such as 1) threshold voltage drop, 2) non-restoring, 3) backdriving, 4) dynamic, 5) diffusion input



Explain the meaning for each of the above five drawbacks. Why are they not good for circuit design and How can you avoid the drawbacks?

3.2. (5%) Comment on conventional CMOS logic circuit with pull-down nMOS network and pull-up pMOS network. Does CMOS logic circuit violate the above circuit design criteria?

3.3. (10%) Design a robust D-latch circuit that does not have any drawback mentioned above.