國立中山大學九十八學年度第二學期資工系數位系統期末考試

學號：　　姓名：

一、選擇與是非題（每題 3 分，12 分）

(　　) 1. 下列何者錯誤？①latch is level triggered ②flip-flop is edge triggered ③area of latch > area of flip-flop ④For a D flip-flop, *D* input must be no change after the application of the positive *Clk* pulse. The time is called hold time。

(　　) 2. 下列那一種記憶元件的讀寫速度最快且所需面積最大？①register file ②SRAM ③DRAM ④Flash memory。

(　　) 3. 下列何者屬於 volatile memory？①DRAM ②ROM ③ EEPROM ④ Flash memory。

(　　) 4. A *k*-bit ring counter circulates a single bit among the flip-flops to provide *k* distinguishable states, and a *k*-bit switch-tail ring counter will go through a sequence of 2*k* distinguishable states.

二、問答題（98 分）

1. Derive the following terms for the sequential circuit shown in Fig. 1.
(1) Input (Excitation) equations (5%)
(2) State equations and output equation (6%)
(3) State table (8%)
(4) State diagram (6%)

2. Design the synchronous sequential circuit using JK flip-flops with the state diagram as shown in Fig. 2.
(1) Complete the state table as shown in Table 1. (8%)
(2) Derive the simplified flip-flop input (excitation) equations. (6%)
(3) Complete the logic diagram as shown in Fig. 3. (5%)

3. Design a four-bit count down binary (synchronous) counter using T flip-flops as shown in Fig. 4.
(1) Complete the state table as shown in Table 2. (7%)
(2) Derive the simplified flip-flop input (excitation) equations. (8%)
(3) Complete the logic diagram as shown in Fig. 4. (6%)

4. Please answer the problems about RAM.
(1) Briefly explain the read and write operations of the 4 × 4 RAM and the memory cell as shown in Fig. 5(a) and 5(b), respectively. (10%)
(2) Explain the address multiplexing for a 64K DRAM as shown in Fig. 6. (8%)

5. Using a 3 × 4 × 2 PLA shown in Fig. 7, implement the truth table shown in Table 3. (15%)

Table 3

A	*B*	*C*	F_1	F_2
0	0	0	0	1
0	0	1	0	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	0

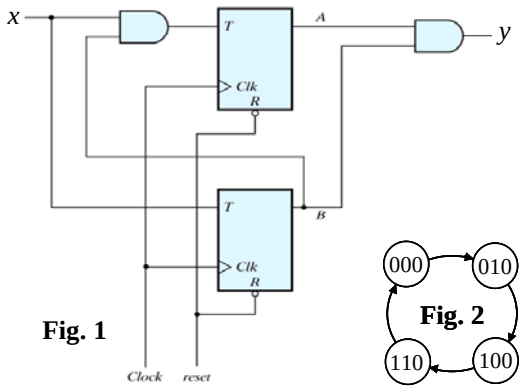

Fig. 1

Fig. 2

Table 1

Present State			Next State			Flip-Flop Inputs					
A	*B*	*C*	*A*	*B*	*C*	J_A	K_A	J_B	K_B	J_C	K_C

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Table 2

Present State				Next State				Flip-flop Inputs			
A_3	A_2	A_1	A_0	A_3	A_2	A_1	A_0	T_{A3}	T_{A2}	T_{A1}	T_{A0}
1	1	1	1	1	1	1	0				
1	1	1	0	1	1	0	1				
1	1	0	1	1	1	0	0				
1	1	0	0	1	0	1	1				
1	0	1	1	1	0	1	0				
1	0	1	0	1	0	0	1				
1	0	0	1	1	0	0	0				
1	0	0	0	0	1	1	1				
0	1	1	1	0	1	1	0				
0	1	1	0	0	1	0	1				
0	1	0	1	0	1	0	0				
0	1	0	0	0	0	1	1				
0	0	1	1	0	0	1	0				
0	0	1	0	0	0	0	1				
0	0	0	1	0	0	0	0				
0	0	0	0	1	1	1	1				

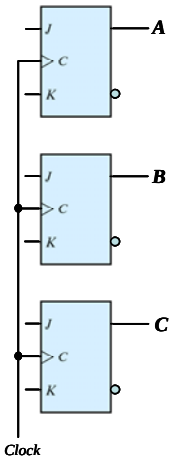

Fig. 3

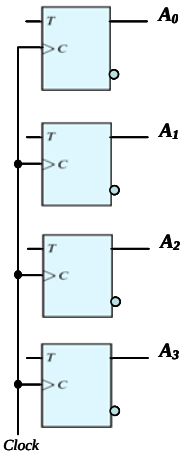

Fig. 4

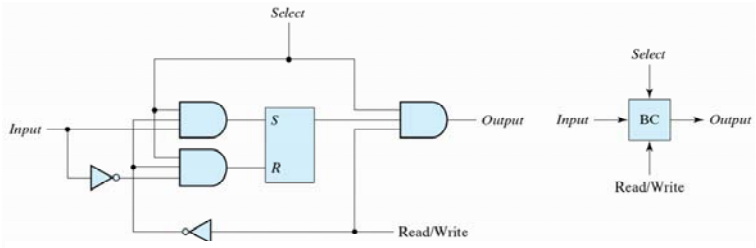

Fig. 5(b)

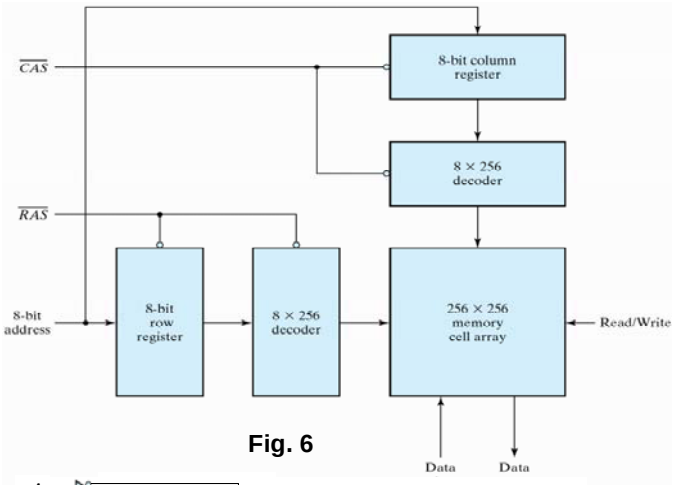

Fig. 6

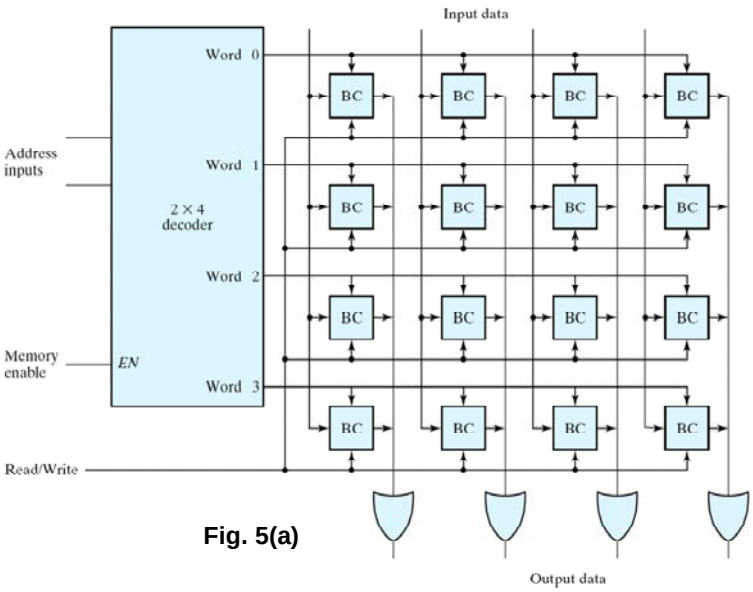

Fig. 5(a)

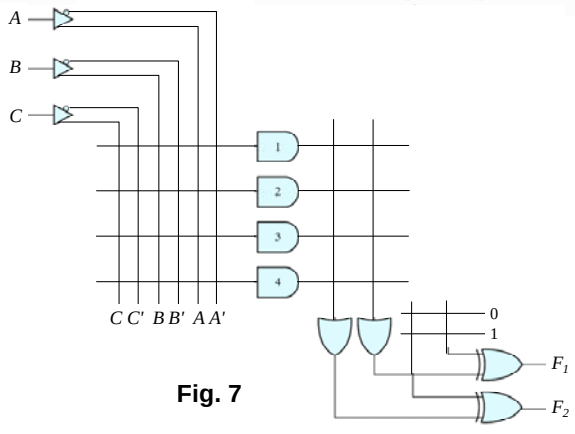

Fig. 7