Computer Organization
Final Exam

1. The following problems refer to the following sequence of instructions:

```
lw    $5, 40($6)
add   $6, $2, $2
sw    $6, 50($1)
```

(1) Indicate dependences and their type. **(5 Points)**

(2) Assume there is no forwarding in this pipelined processor. Indicate hazards and add **"nop"** instructions to eliminate them. **(5 Points)**

2. This question examines the accuracy of various branch predictors for the following repeating pattern of branch outcomes.

Branch outcomes
T, T, NT, T

(1) What is the accuracy of always-taken and always-not-taken predictors for this sequence of branch outcomes? **(5 Points)**

(2) What is the accuracy of the two-bit predictor for the first four branches in this pattern, assuming that the predictor starts off in the bottom left state from **Figure 1**. **(5 Points)**

(3) What is the accuracy of the two-bit predictor if this pattern is repeated forever? **(5 Points)**

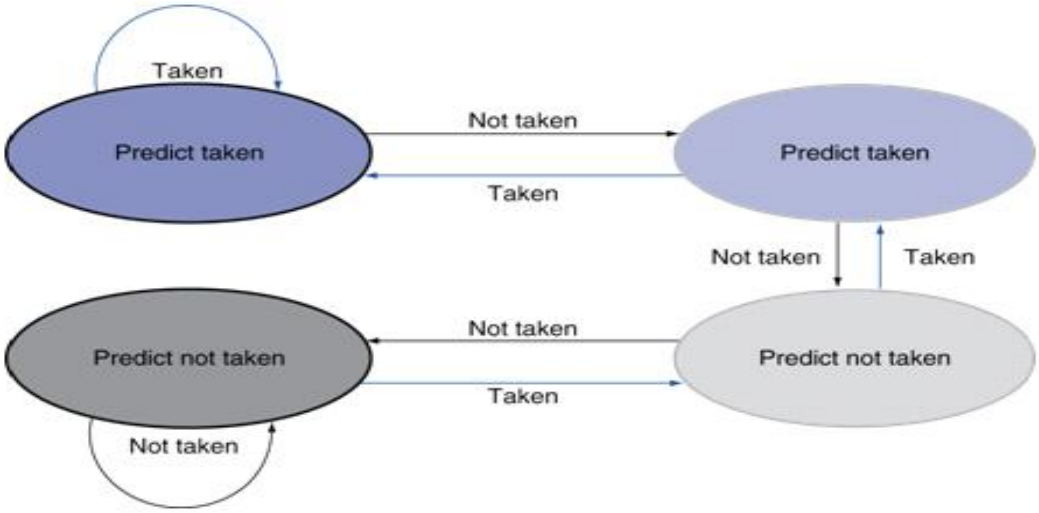

Figure 1

3. For a direct-mapped cache design with 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-4	3-0

(1) What is the cache line size (in words)? **(5 points)**

(2) How many entries does the cache have? **(5 points)**

(3) What is the ratio between total bits required for such a cache implementation over the data storage bits? **(5 points)**

4. Please refer to the execution of the instruction **"`slt $2, $1, $3`"** in the pipelined data path from **Figure 2.**

(1) For each stage of the pipeline, what are the values of control signals asserted by this instruction in that pipeline stage? **(7 Points)**

EX	**MEM**	**WB**
ALUSrc = _____ ALUOp = 10 RegDst = _____	Branch = _____ MemWrite = _____ MemRead = _____	MemtoReg = _____ RegWrite = _____

(1) How much time does the control unit have to generate the ALUSrc control signal? Compare this to a single-cycle organization. **(5 Points)**

(2) What is the value of the PCSrc signal for this instruction? **(3 Points)**

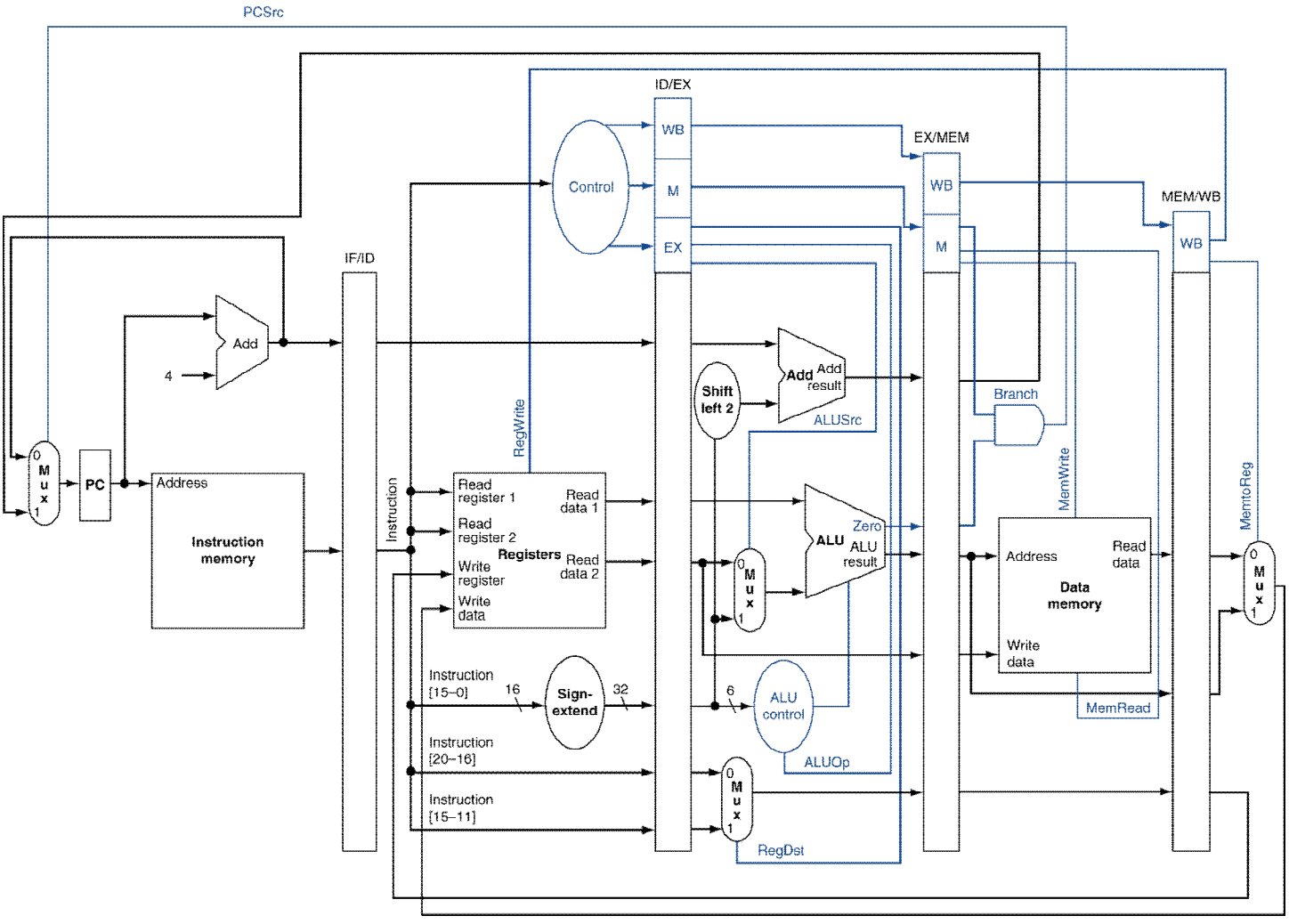

Figure 2

5. Assume that the breakdown of dynamic instructions into various instruction categories is as follows:

R-Type	beq	jmp	lw	sw
50%	15%	10%	15%	10%

Also, assume the following branch predictor accuracies:

Always-taken	Always-not-taken	2-bit
40%	60%	80%

(1) Stall cycles due to mispredicted branches increase the CPI. What is the extra CPI due to mispredicted branches with the always-taken predictor? Assume that branch outcomes are determined in the EX-stage, that there are no data hazards, and that no delay slots are used. **(5 Points)**

(2) Repeat (1) for the "always-not-taken" predictor. **(5 Points)**

(3) Repeat (1) for the 2-bit predictor. **(5 Points)**

6. There are three small caches, each consisting of four one-word blocks. One cache is fully associative, a second is two-way set associative, and the third is direct-mapped. Find the numbers of misses for each organization given the following sequence of block addresses: **0, 8, 0, 6, 8**. Assume that the least recently used replacement policy for the set-associative cache. **(10 Points)**

7. Below is a list of 32-bit memory address reference, given as "**byte addresses**".

Address	24	856	700	856	24	336	260	696	256	420	340	860

(1) Given a direct-mapped cache with 16 one-word blocks. List if each reference is a hit or a miss, assuming the cache is initially empty. **(5 Points)**

(2) There are three direct-mapped cache designs possible, all with a total of eight words of data: C1 has one-word blocks, C2 has two-word blocks, and C3 has four-word blocks. In terms of miss rate, which cache design is the best? If the miss stall time is 25 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles, and C3 takes 5 cycles, which is the best cache design? **(5 Points)**

8. Media applications that play audio or video files are part of a class of workloads called "streaming" workloads; i.e., they bring in large amounts of data but do not reuse much of it. Consider a video streaming workload that accesses a 512 KB working set sequentially with the following address stream:

Address	0	4	8	12	16	20	24	28	32…

Assume a 64 KB direct-mapped cache with a 32-byte line. What is the miss rate for the address stream above? How is this miss rate sensitive to the size of the cache or the working set? How would you categorize the misses this workload is experiencing, based on the 3C model. **(5 Points)**

9. Consider a virtual memory system with the following properties:

A. 64-bits virtual addresses size

B. 16-KB page size

C. 8 bytes page table entry size

What is the total size of the page table for each process on this machine? **(5 Points)**

10. (1) What's the main concept of pipelining in computer organization? **(2 Points)**
(2) What are the major design challenges of pipelining? **(2 Points)**
(3) What are the major techniques to solve the challenges? **(3 Points)**

11. What's the main idea of loop unrolling? **(2 Points)**. List at least two aspects that the loop unrolling can help to improve performance? **(3 Points)**

12. What is the major similarity between the concept of cache and the concept of virtual memory? **(3 Points).** What is the major difference between them? **(3 Points)**

13. Compare the advantage and disadvantage of the write-back and write-through policies for cache. **(2 Points)**