國立中山大學九十七學年度第二學期資工系數位系統期末考試題

學號：　　姓名：

一、選擇與是非題（每題 4 分，40 分）

( ) 1. What kind of flip-flop is the most popular component to compose a register? ①*SR* ②*D* ③*JK* ④*T*

( ) 2 What kind of flip-flop is the most popular component to compose an asynchronous counter? ①*SR* ②*D* ③*JK* ④*T*。

( ) 3. Compared with a synchronous counter, which one is the main weakness of the asynchronous counter? ①longer delay ②larger cost (area) ③larger power consumption ④more difficult to design

( ) 4. What kind of storage component usually merges the input data bus and output data bus into a bi-direction I/O bus to reduce the number of I/O pins? ①Register file ②ROM ③RAM ④FIFO

( ) 5. How many address lines are required in a 16M×16 RAM? ①16 ②20 ③24 ④28

( ) 6. The BCD counter can be achieved by a 4-bit up/down counter with parallel load. The '0' must be loaded when count direction is down and counter content is 9.

( ) 7. To extend the address space (increase the number of memory words), a larger RAM can be composed of some smaller RAMs with parallel connection (並聯).

( ) 8. Compared with RAM, register file has shorter access time and smaller capacity (memory words).

( ) 9. The control unit in a digital system is a sequential circuit and it can be regarded as a finite state machine (FSM).

( ) 10. The datapath in a digital system is a combinatorial circuit.

二、問答題（80 分）

1. Derive (a) excitation equations, (b) a next-state equation, (c) a state/output table, and (d) a state diagram for the circuit shown in Fig. 1. (18%)

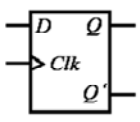
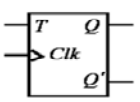
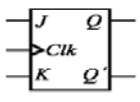
2. Using the synthesis procedure for FSM models, design a synchronous counter that counts in the sequence 0, 1, 3, 5, 0, 1, 3, 5, …, using natural binary encoding as shown in Fig. 2 and: (a) D flip-flops (b) JK flip-flops. (18%)

3. Design a 4-bit register that can load new data and swap the most-significant and least-significant bits as shown in Table 1. (10%)

4. Construct a 4-bit asynchronous counter using: (a) T flip-flops (b) D flip-flops. (12%)

5. (1) Please fill in the blanks in Table 2 with the control words of one's counter example. (14%)

(2) Please describe the operation of the datapath shown in Fig. 3 to perform Ocount := 0 and Ocount := Ocount + Temp. (8%)

Flip–flop name	*Flip–flop symbol*	*Characteristic table*	*Characteristic equation*	*Excitation table*
D		D | $Q(next)$ 0 | 0 1 | 1	$Q(next) = D$	Q | $Q(next)$ | D 0 0 0 0 1 1 1 0 0 1 1 1
T		T | $Q(next)$ 0 | Q 1 | Q'	$Q(next) = TQ' + T'Q$	Q | $Q(next)$ | T 0 0 0 0 1 1 1 0 1 1 1 0
JK		J K | $Q(next)$ 0 0 | Q 0 1 | 0 1 0 | 1 1 1 | Q'	$Q(next) = JQ' + K'Q$	Q | $Q(next)$ | J K 0 0 | 0 X 0 1 | 1 X 1 0 | X 1 1 1 | X 0

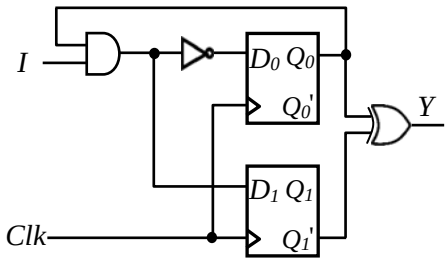


Fig. 1

S_1	S_0	Operation	Next State
0	X	No Change	$Q_3\,Q_2\,Q_1\,Q_0$
1	0	Load Input	$I_3\ I_2\ I_1\ I_0$
1	1	Swap	$Q_1\,Q_0\,Q_3\,Q_2$

Table 1

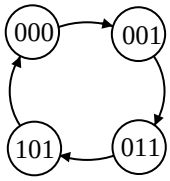


Fig. 2

Control Words	IE	Write address	Read address A	Read address B	ALU operation	Shifter operation	OE
1	1	R1	X	X	X	X	0
2	0	R3	R0	R0	add	pass	0
3	0						0
4	0						0
5	0						0
6	0						0
7	0	none	R3	0	add	pass	1

Table 2

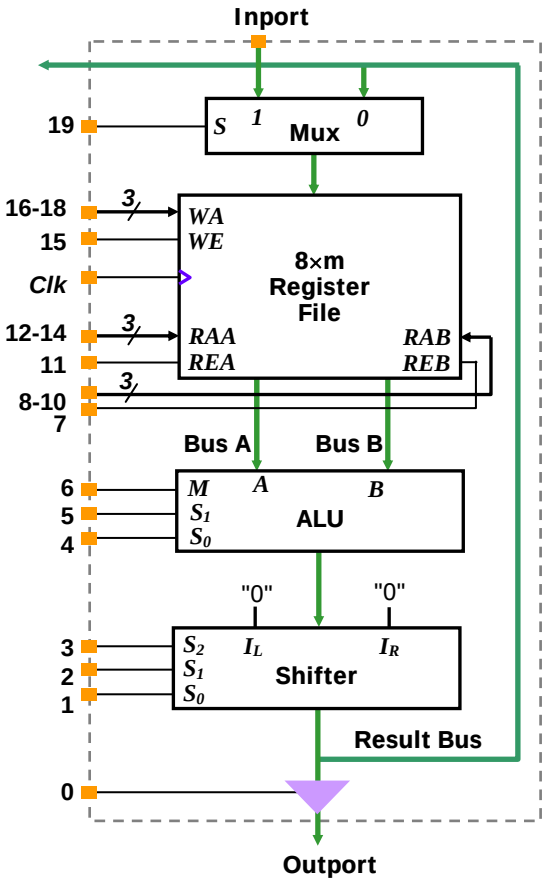


Fig. 3

1. Data := Inport
2. Ocount := 0
3. Mask := 1
   while Data ≠ 0 repeat
4. Temp := Data AND Mask
5. Ocount : = Ocount + Temp
6. Data := Data >> 1
   end while
7. Output := Ocount

Data => R1
Mask => R2
Ocount => R3
Temp => R4

S_2	S_1	S_0	*Shift Operations*
0	0	0	pass
0	0	1	pass
0	1	0	not used
0	1	1	not used
1	0	0	shift left
1	0	1	rotate left
1	1	0	shift right
1	1	1	rotate right

M	S_1	S_0	*ALU Operations*
0	0	0	complement A
0	0	1	AND
0	1	0	EX−OR
0	1	1	OR
1	0	0	decrement A
1	0	1	add
1	1	0	subtract
1	1	1	increment A