國立中山大學102學年度第一學期資工系數位系統期末考試

學號：　　姓名：

一、選擇與是非題（每題3分，12分）

(　　) 1. How many address lines are required in a 1G×32 RAM? ①9 ②30 ③32 ④35

(　　) 2. The clock inputs of all flip-flops in binary ripple counter receive a common clock.

(　　) 3. SRAM is the non-volatile memory.

(　　) 4. Programmable read-only memory (PROM) has fixed AND array and programmable OR array.

二、問答題（90分）

1. Derive the following terms for the sequential circuit shown in Fig. 1.
(1) Input (Excitation) equations (4%)　(2) State equations (6%)
(3) State table (Table 1) (4%)　(4) State diagram (4%)

2. Design a sequential circuit with two JK flip-flops *A* and *B* and two inputs *E* and *F*. If *E*=0, the circuit remains in the same state regardless of the value of *F*. When *E*=1 and *F*=1, the circuit go through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When *E*=1 and *F*=0, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats.
(1) Complete the state table and JK flip-flop input as shown in Table 2. (8%)
(2) Derive the simplified flip-flop input (excitation) equations using the K-map. (12%)
(3) Draw the logic diagram with JK flip-flops as shown in Fig. 2. (6%)

3. Design a counter with *T* flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Assume that binary states 010 and 101 are considered as don't care conditions.
(1) Complete the state table as shown in Table 3. (6%)
(2) Derive the simplified flip-flop input (excitation) equations. (6%)
(3) The counter may not operate properly if the unused states are treated as don't care condition. Find a way to correct the design and please explain your way. (4%)

4. Using an 8 × 2 ROM shown in Fig. 3 and a 3 × 4 × 2 PLA shown in Fig. 4, implement the truth table shown in Table 4. (6%) (8%)

5. Please answer the following problems.
(1) Explain the operations of the 4-bit universal shift register shown in Fig. 5 and complete the function table shown in Table 5. (6%)
(2) Explain the read and write operations of the 4 × 4 RAM and the memory cell as shown in Fig. 6(a) and 6(b), respectively. (10%)

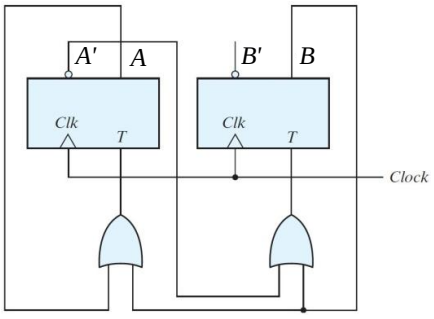

Fig. 1

Table 1

Present state		Next state	
A	*B*	*A*	*B*

Table 3

Present state			Next state			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}

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Fip-flop	D	JK	T
characteristic equation	$Q(t+1) = D$	$Q(t+1) = JQ'+K'Q$	$Q(t+1) = T \oplus Q$

D	Q(t + 1)
0	0
1	1

J	K	Q(t + 1)
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$

T	Q(t + 1)
0	$Q(t)$
1	$Q'(t)$

characteristic table

excitation table

Q(t)	Q(t + 1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q(t)	Q(t + 1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 2

Present state A	Present state B	Inputs E	Inputs F	Next state A	Next state B	Flip-Flop Inputs J_A	Flip-Flop Inputs K_A	Flip-Flop Inputs J_B	Flip-Flop Inputs K_B
0	0	0	0						
0	0	0	1						
0	0	1	0						
0	0	1	1						
0	1	0	0						
0	1	0	1						
0	1	1	0						
0	1	1	1						
1	0	0	0						
1	0	0	1						
1	0	1	0						
1	0	1	1						
1	1	0	0						
1	1	0	1						
1	1	1	0						
1	1	1	1						

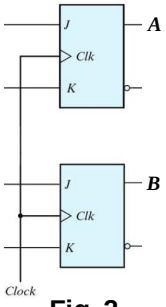

Fig. 2

Table 4

A	B	C	F_1	F_2
0	0	0	1	1
0	0	1	0	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

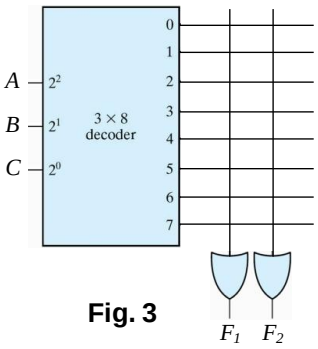

Fig. 3

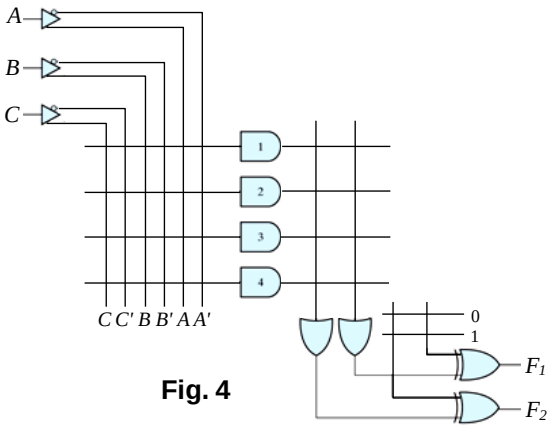

Fig. 4

Table 5

Mode Control s_1	Mode Control s_0	Register Operation
0	0	
0	1	
1	0	
1	1	

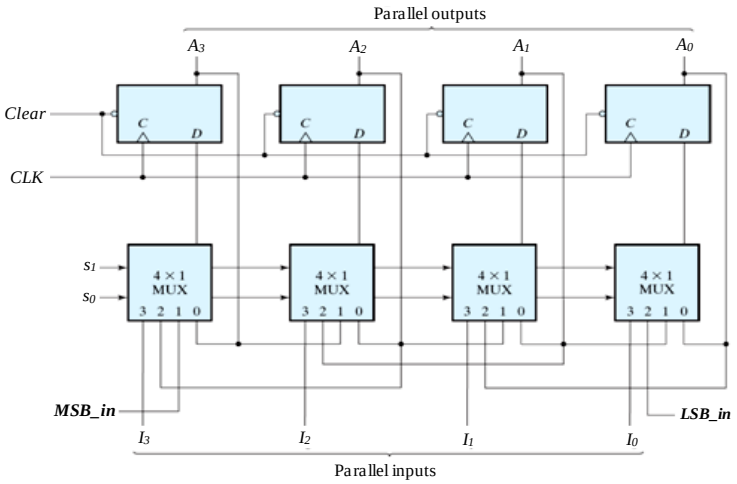

Fig. 5

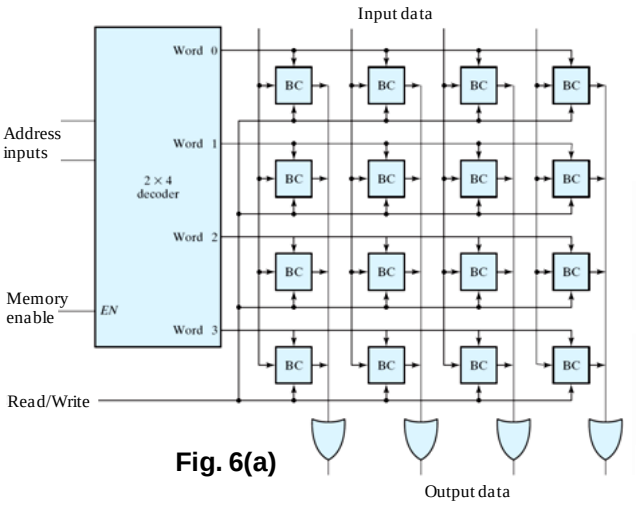

Fig. 6(a)

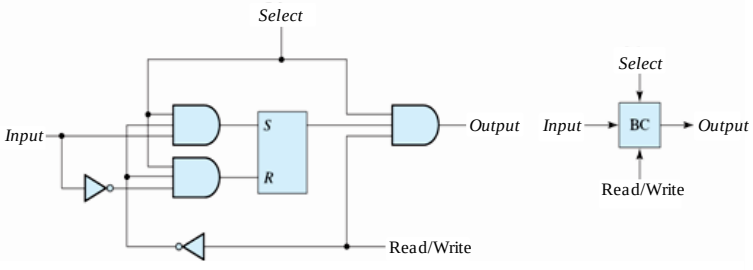

Fig. 6(b)