Digital Electronics Spring 2011 Final Exam 06/27/2011

Name: ID#

Useful parameters and equations:

$\mu_n C_{ox} = 200\mu A/V^2, \quad \mu_p C_{ox} = 100\mu A/V^2,\ V_{THN} = 0.4,\ V_{THP} = -0.4,\ r_o = 1/\lambda I_D$

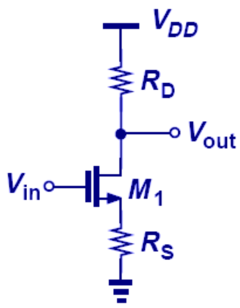
$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})^2\right]$ [Transistor operated at saturation region, $V_{GS}-V_{TH} > 0$ and $V_{DS} > V_{GS}-V_{TH}$]

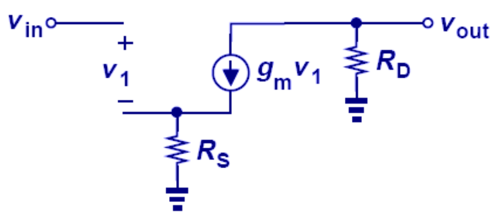
$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$ [Transconductance]

$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})\right]}$ [Transistor on Resistance]

$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$ [Transconductance]

1. In the following CS stage with degeneration circuit, please find the voltage gain. (8%)



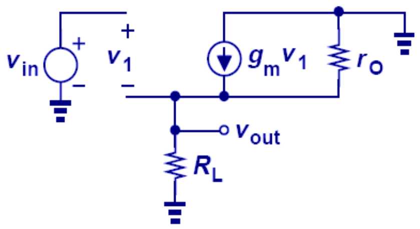


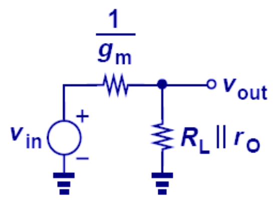
Ans:

$$v_{in} = v_1 + g_m v_1 R_S \Rightarrow v_1 = \frac{v_{in}}{1 + g_m R_S}$$

$$v_{out} = -g_m v_1 R_D \quad \frac{v_{out}}{v_{in}} = -\frac{g_m R_D}{1 + g_m R_S} = -\frac{R_D}{\frac{1}{g_m} + R_S}$$

2. In the following source follower circuit, please find the voltage gain. (8%)



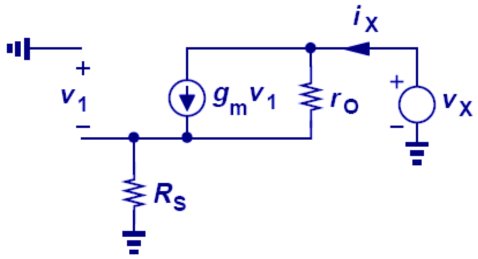


Ans:

$$g_m v_1 (r_O \| R_L) = v_{out} \qquad v_{in} = v_1 + v_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{g_m (r_O \| R_L)}{1 + g_m (r_O \| R_L)} = \frac{r_O \| R_L}{\frac{1}{g_m} + r_O \| R_L}$$

3. In the following CS stage with degeneration circuit, please find the output impedance. (8%)



Ans:

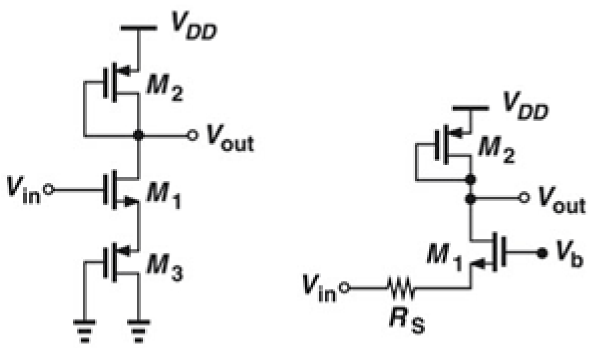
$$i_{r_o} = i_X - g_m v_1 = i_X - g_m(-i_X R_S) = i_X + g_m i_X R_S$$

$$r_O(i_X + g_m i_X R_S) + i_X R_S = v_X$$

$$\frac{v_X}{i_X} = r_O(1 + g_m R_S) + R_S$$

$$= (1 + g_m r_O) R_S + r_O \approx g_m r_O R_S + r_O$$

4. Calculate the voltage gain of the circuits depicted in Figures below. Assume λ = 0. (8%)

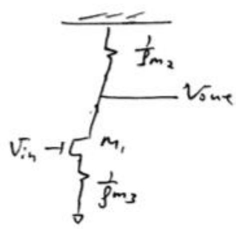


(a) (b)

Ans:

a). Equivalent circuit is:

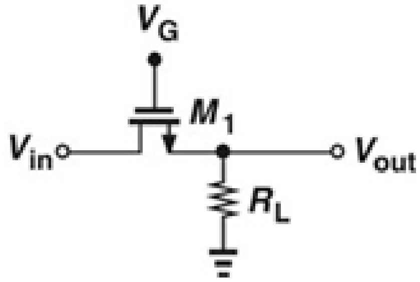
$$\therefore \; A_v = - \frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}}}$$



(c) Referring to Eq. (7.109) with $R_D = \frac{1}{g_{m2}}$ and $g_m = g_{m1}$, we have

$$A_v = \boxed{\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}} + R_S}}$$

5. In the following circuit, M_1 serves as an electronic switch. If V_{in}=0, determine W/L such that the circuit attenuates the signal by only 10%. Assume V_{in}=0, and R_L=200. (8%)

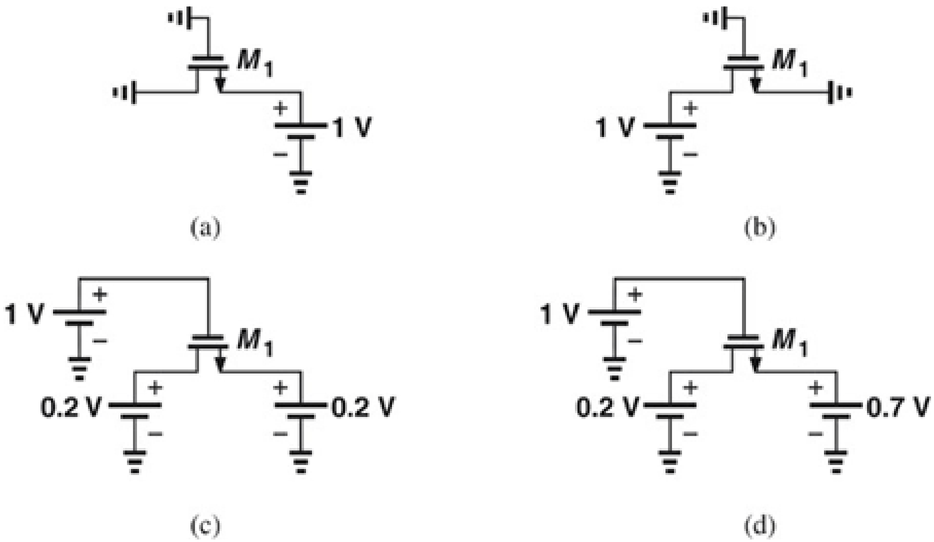


Ans:

$$V_{out} = 0.9V_{in} = \frac{R_L}{R_{on} + R_L} V_{in} \Rightarrow R_{on} = 22.2$$

$$\frac{W}{L} = \frac{1}{\mu_n C_{ox}(V_{GS} - V_{TH})R_{on}} = \frac{1}{200u(1.8 - 0.4)(22.2)} = 160.87$$

6. Determine the region of operation of M_1 in each of the circuits shown below. (8%)



20. (a) OFF ∵ $V_{GS} = 0$ ($V_{GS} < V_{TH}$)

(b) OFF ∵ $V_{GS} = 0$ ($V_{GS} < V_{TH}$)

(c) TRIODE (LINEAR) ∵ $V_{GS} > V_{TH}$ &
$V_{DS} \ll 2(V_{GS} - V_{TH})$

(d) SATURATION ∵ $V_{GS} > V_{TH}$ & $V_{DS} > V_{GS} - V_{TH}$

7. An NMOS device carries 1 mA with $V_{GS}-V_{TH}=0.6$ V and 1.6 mA with $V_{GS}-V_{TH}=0.8$ V. If the device operates in the triode region, calculate V_{DS} and W/L. (8%)

Ans:

7. Given : NMOS $I_D = 1mA$ $V_{GS}-V_{TH}=0.6V$

$I_D = 1.6mA$ $V_{GS}-V_{TH}=0.8V$

(triode region) $\mu_n C_{ox} = 200\frac{\mu A}{V^2}$

Find V_{DS} & W/L.

$$1mA = \mu_n C_{ox}\frac{W}{L}\left[(0.6)V_{DS} - V_{DS}^2/2\right] \quad \text{——} ①$$

$$1.6mA = \mu_n C_{ox}\frac{W}{L}\left[(0.8)V_{DS} - V_{DS}^2/2\right] \quad \text{——} ②$$

$$② \div ① : 1.6 = \frac{0.8V_{DS} - V_{DS}^2/2}{0.6V_{DS} - V_{DS}^2/2} = \frac{1.6 - V_{DS}}{1.2 - V_{DS}}$$

$$\Rightarrow V_{DS} = \frac{1.6(0.2)}{0.6} \approx 0.533\ V$$

$$\Rightarrow \frac{W}{L} = \frac{I_D}{\mu_n C_{ox}\left[(V_{GS}-V_{TH})V_{DS} - V_{DS}^2/2\right]}$$

$$= \frac{1mA}{200\frac{\mu A}{V^2}\left[(0.6V)(0.533V) - (0.533V)^2/2\right]}$$

$$\approx 28.$$

8. An NMOS device with $\lambda=0.1V^{-1}$ must provide a $g_m r_o$ of 20 with V_{DS}=1.5V. Determine the required value of W/L if I_D=0.5mA . (8%)

Ans:

36. Given NMOS with $\lambda = 0.1\ V^{-1}$ $g_m r_o = 20$

$V_{DS} = 1.5V$

determine W/L if $I_D = 0.5mA$.

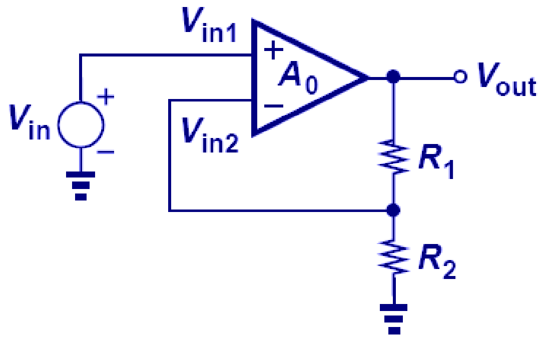
$$r_o = \frac{1}{\lambda I_D} = \frac{1}{(0.1V^{-1})(0.5mA)} = 20\ k\Omega$$

$$\Rightarrow g_m = \frac{20}{20k\Omega} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$

$$\therefore \frac{W}{L} = \left(\frac{20}{20k\Omega}\right)^2 \frac{1}{2\mu_n C_{ox} I_D}$$

$$= \left(\frac{1}{1k\Omega}\right)^2 \frac{1}{2\left(200\frac{\mu A}{V^2}\right)(0.5mA)} \approx 5.$$

9. (a) Please find the closed loop gain of a noninverting amplifier shown below. (Assuming infinite gain A_0)
(b) The noninverting amplifier employs an op amp having a nominal gain of 5000 to achieve a nominal closed-loop gain of 8. Determine the gain error which is the close loop gain found in part (a) multiply by the inverse of the nominal gain of op. (8%)

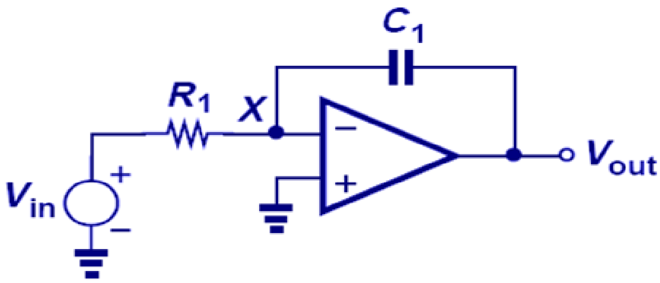


Ans:

(a) $V_{in2} = \dfrac{R_2}{R_1+R_2}V_{out}$ $\quad V_{in2} \approx V_{in1} \approx \dfrac{R_2}{R_1+R_2}V_{out}$ $\quad \dfrac{V_{out}}{V_{in}} = \dfrac{R_1+R_2}{R_2} = 1+\dfrac{R_1}{R_2}$

(b) $\text{closed}-\text{loop gain} = (1+\dfrac{R_1}{R_2}) = 8$ $\quad \text{gain error} = (1+\dfrac{R_1}{R_2})(A_0)^{-1} = \dfrac{8}{5000} = 0.16\%$

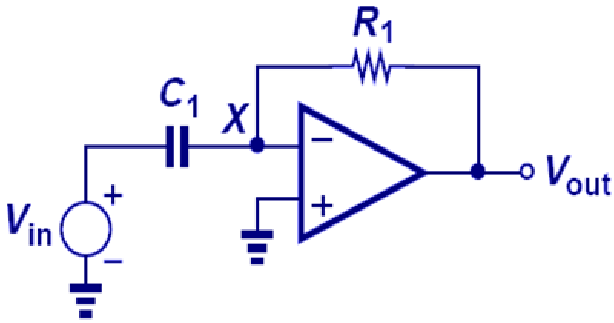
10. (a) Please find the closed loop gain of a integrator shown below. The integrator is used to amplify a sinusoidal input by a factor of 10. If $A_0=\infty$ and $R_1C_1 = 25$ ns, compute the frequency of the sinusoid. (8%)



(a) $$\frac{V_{out}}{V_{in}} = -\frac{\frac{1}{C_1 s}}{R_1} = -\frac{1}{R_1C_1 s}$$

(b) $$\frac{1}{RC\omega} = 10 \Rightarrow \frac{1}{\omega} = 10\times 25ns \Rightarrow \omega = 4MHz$$

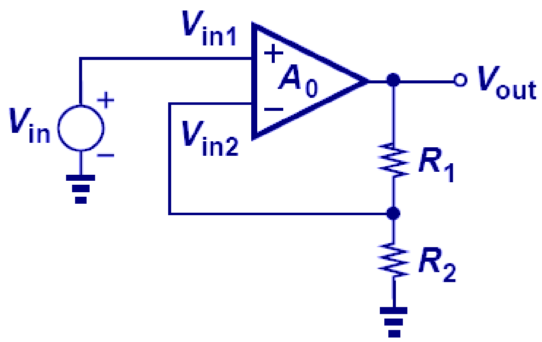
11. (a) Please find the closed loop gain of a differentiator shown below. (b) The differentiator of Fig. 8.52 is used to amplify a sinusoidal input at a frequency f = 1 MHz by a factor of 5. If A_0=∞, determine the value of R_1C_1. (8%)



(a) $$\frac{V_{out}}{V_{in}} = -\frac{R_1}{\frac{1}{C_1 s}} = -R_1C_1s$$

(b) $$A_V = \frac{R_1}{\frac{1}{\omega C_1}} = \omega R_1 C_1 = 5 \Rightarrow R_1C_1 = \frac{5}{\omega} = \frac{5}{2\pi \times 10^6} = 7.958 \times 10^{-7}$$

12. A noninverting amplifier with a nominal gain of 4 senses a sinusoid having a peak amplitude of 0.5 V. If the op amp provides a slew rate of 1 V/ns, what is the highest input frequency for which no slewing occurs? (8%)



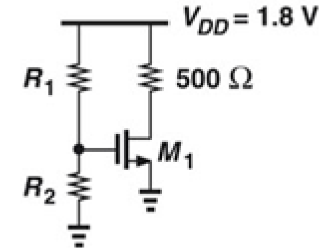
$$V_{in}(t) = 0.5 \sin \omega t \Rightarrow V_{out} = 0.5 \times (1 + R_1 / R_2) \sin \omega t$$

$$\frac{dV_{out}}{dt} = 0.5(1 + R_1 / R_2)\omega \cos \omega t = \text{maximum when } \cos \omega t = 1$$

$$\Rightarrow \frac{dV_{out}}{dt}\Big|_{\max} = 0.5\omega(1 + R_1 / R_2) = 2\omega \quad \text{where nominak gain } (1 + R_1 / R_2) = 4$$

$$\text{Therefore, highest frequency} \Rightarrow 2\omega = 1V / ns \Rightarrow \omega = 0.5 rad / ns \Rightarrow f_{MAX} \approx 79.6 MHz$$

13. We wish to design a drain current of 1 mA. If $W/L = 20/0.18$, compute **(a)** R_1 and **(b)** R_2 such that input impedance is at least 20 kΩ. Assume $\mu_n C_{ox} = 200\ \mu A/V^2$ and $V_{TH} = 0.4$ V. (8%)



Ans:

② To get $I_{DS} = 1$ mA.

$\frac{1}{2} \mu C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 = 1 \times 10^{-3}$ A.

$\frac{1}{2} (200 \times 10^{-6}) \left(\frac{20}{0.18}\right) (V_{GS} - V_{TH})^2 = 10^{-3}$

$(V_{GS} - V_{TH})^2 = 0.09$

$V_{GS} - V_{TH} = 0.3,$

ie. $V_{GS} = 0.7.,$

Since $V_{GS} = \frac{R_2}{R_1 + R_2} \times 1.8$

$0.7 = \frac{R_2}{R_1 + R_2} \times 1.8$

$0.7 R_1 = \cdot R_2,$

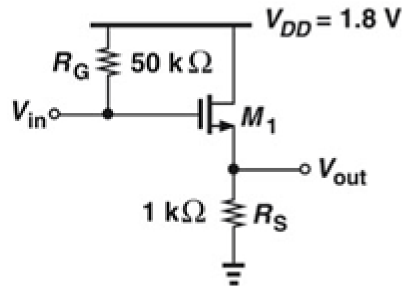
$\therefore \frac{R_1}{R_2} = \frac{11}{7}.$ ——— ①

To get input impedance ≥ 20k.

$R_1 // R_2 \geq 20$ kΩ. ——— ②

By inspection, setting $R_1 = 55$ kΩ and $R_2 = 35$ kΩ will satisfy both ① and ②.

14. The source follower shown below is biased through R_G. Calculate the voltage gain if $W/L = 20/0.18$ and $\lambda = 0.1 V^{-1}$. Assume $\mu_n C_{ox} = 200\ \mu A/V^2$, $V_{TH} = 0.4$ V. (8%)



7.49

$$V_{GS} = V_{DS}$$

$$V_{GS} = V_{DD} - I_D R_S = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 (1 + \lambda V_{GS}) R_S$$

$$V_{GS} = V_{DS} = 0.7036 \text{ V}$$

$$I_D = 1.096 \text{ mA}$$

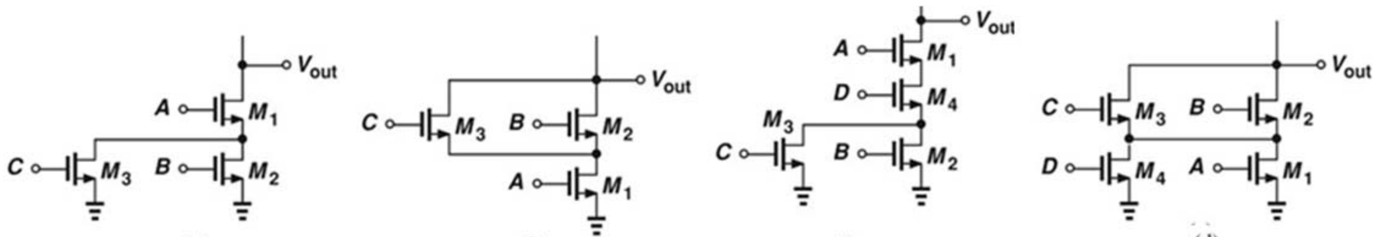
$$A_v = \frac{r_o \parallel R_S}{\frac{1}{g_m} + r_o \parallel R_S}$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D} = 6.981 \text{ mS}$$

$$r_o = \frac{1}{\lambda I_D} = 9.121 \text{ k}\Omega$$

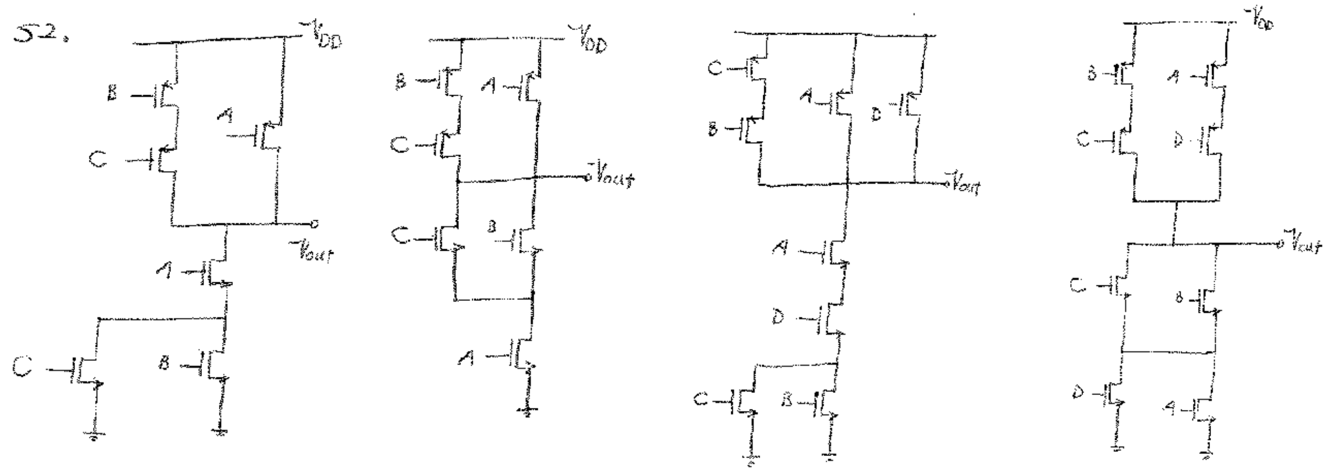
$$A_v = \boxed{0.8628}$$

15. For each NMOS section shown below, draw the dual PMOS section, construct the overall CMOS gate, and determine the logical function performed by the gate. (8%)



(a) (b) (c) (d)

S2.



$V_{out} = \overline{(B+C)A}$ $V_{out} = \overline{(B+C)\cdot A}$ $V_{out} = \overline{(B+C)D\cdot A}$ $V_{out} = \overline{(A+D)\cdot(B+C)}$