Chapter Exam

Appendix C-The Basics of Logic Design

2011/03/15

1. Prove that the two equations E1, E2 are equivalent by DeMorgan's theorem. **(10 Points)**
E1 = ((A · B) + (A · C) + (B · C)) · $\overline{(A \cdot B \cdot C)}$
E2 = (A · B · $\overline{C}$) + (A · C · $\overline{B}$) + (B · C · $\overline{A}$)

2. Prove that the NOR gate is universal by showing how to build the AND, OR, and NOT functions using a two-input NOR gate. **(10 Points)**

3. Assume that X consists of 2 bits, x1 x0, and Y consists of 2 bits, y1 y0. Write logic functions that are true if and only if
(1) X < Y, where X an Y are thought of as unsigned binary numbers. **(10 Points)**
(2) X < Y, where X an Y are thought of as signed (two's complement) numbers. **(10 Points)**
(3) X = Y. **(10 Points)**

4. A friend would like you to build an "electronic eye" for use as a fake security device. The device consists of three lights lined up in a row, controlled by the outputs Left, Middle, and Right, which, if asserted, indicate that a light should be on. Only one light is on at a time, and the light "moves" from left to right and then from right to left. Note that the rate of the eye's movement will be controlled by the clock speed (which should not be too great) and that there are essentially no inputs.
(1) Draw the graphical representation for the finite-state machine used to specify the electronic eye. **(10 Points)**
(2) Assign state numbers to the states of the finite-state machine you constructed and write a set of logic equations for each of the outputs, including the next-state bits. **(10 Points)**

5. Derive the logic equations (5a, 5b, 5c, 5d and 5e) of a 16-bit carry-lookahead adder in Fig 2. There is no need to simplify the equations. **(10 Points)**
gi = ai · bi pi = ai + bi
P0 = p3 · p2 · p1 · p0
P1 = p7 · p6 · p5 · p4
P2 = p11 · p10 · p9 · p8
P3 = [5a]

G0 = g3 + (p3 · g2) + (p3 · p2 · g1) + (p3 · p2 · p1 · g0)
G1 = g7 + (p7 · g6) + (p7 · p6 · g5) + (p7 · p6 · p5 · g4)
G2 = [5b]
G3 = [5c]

C1 = G0 + (P0 · c0)

C2 = G1 + (P1 · G0) + (P1 · P0 · c0)

C3 = 5d

C4 = 5e

6. One simple way to model time for logic is to assume each AND or OR gate takes the same time for a signal to pass through it. Time is estimated by simply counting the number of gates along the path through a piece of logic. Compare the number of *gate delays* for paths of two 16-bit adders, one using the ripple carry as Fig 1 and one using the two-level carry lookahead as Fig 2. **(10 Points)**

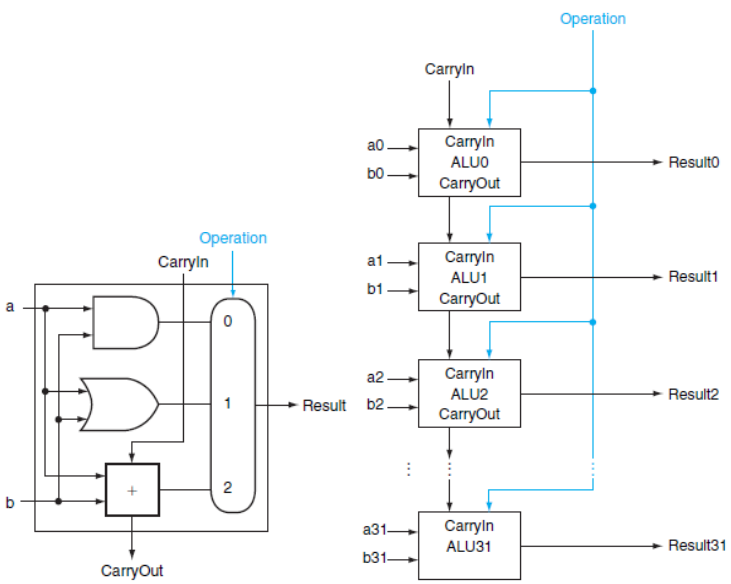

Fig. 1

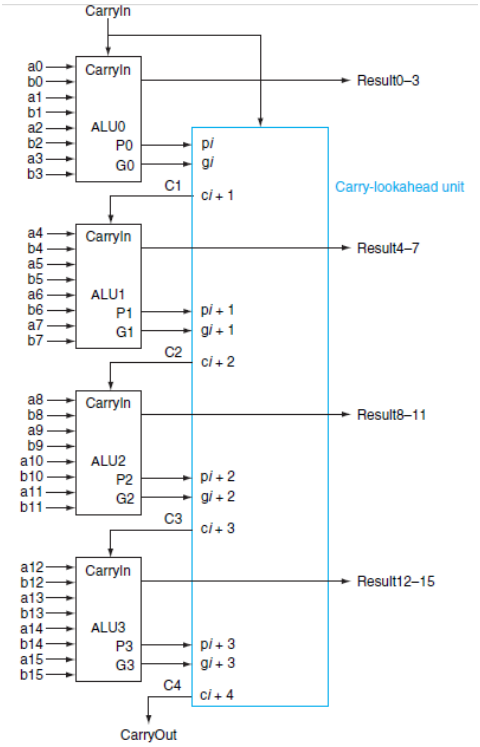

Fig. 2

7. One D flip-flop with a falling trigger is implemented by two D latches and one NOT gate. The D flip-flop has two input signals, C (clock) and D (data) and one output signal (Q). Please draw the block diagram for a D flip-flop with a falling trigger. In addition, please draw a timing diagram (waveform) to show how the D-flip-flop changes its internal signal (the signal between the two D latches) and its output signal Q. **(10 Points)**

8. Both the register file and the SRAM are built with D-latches. What are the differences between the register file and the SRAM? **(5 Points)**

9. Please compare the advantages and disadvantages of a PLA (programmable logic array) and a ROM (read only memory). **(5 Points)**

Chapter Exam

Chapter 1-Computer Abstractions and Technology

2011/03/29

10. Consider the following performance measurements of a program, which computer has the higher MIPS rating? **(10 Points)**

Measurement	Computer A	Computer B
Instruction count	10 billion	8 billion
Clock rate	4 GHz	4GHz
CPI	1	2

11. Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.

	Clock rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	1.4 GHz	1	2	3	4
P2	2 GHz	2	2	2	2

(1) Given a program with 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C and 20% class D, which implementation is faster? **(10 Points)**

(2) Which is the global CPI for each implementation? **(10 Points)**

12. The following table shows results for SPEC2006 benchmark programs running on an AMD Bracelona.

Name	Intr. Count x10^9	Execution time (seconds)	Reference time (seconds)
perl	2118	500	9770

(1) Find the CPI if the clock cycle time is 0.333 ns. **(10 Points)**

(2) Find the SPEC ration. **(10 Points)**

13. The table below shows instruction-type breakdown for some program.

# Instructions				
Compute	Load	Store	Branch	Total
1000	400	100	50	1550

(1) Assuming that computes take 1 cycle, loads and store instructions take 2 cycles, and branches take 2 cycles, find the execution time of this program on a 3 GHz MIPS processor. **(10 Points)**

(2) Assuming that computes take 1 cycle, loads and store instructions take 2 cycles, and branches take 2 cycles, what is the speed-up of this program if the number of compute instruction can be reduced by one-half? **(10 Points)**

14. Consider two different processor P1 and P2 executing the same instruction set with the clock rates and CPIs given in the following table.

Processor	Clock Rate	CPI
P1	1.5 GHz	1.0
P2	3 GHz	2.5

(1) Which processor has the highest performance? **(10 Points)**

(2) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions. **(10 Points)**

(3) We are trying to reduce the time by 10% but this leads to an increase of 20% in the CPI. What clock rate (for each processor) should we have to get this time reduction? **(10 Points)**

Chapter Exam

Chapter 2 Instructions: Language of the computer

2011/04/19

15. What's the difference between the **"MOV"** instruction and the **"LDR"** instruction in ARM CPU? **(5 Points)**

16. Prove that " –x = x' + 1" in 2's complement representation. **(5 Points)**

17. A recursive C language statement is as:

```
int fact(int n)
{
    if(n<1) return (1);
    else return(n*fact(n-1));
}
```

The corresponding MIPS assembly code is as:

```
fact:  addi $sp, $sp, -8
       sw   $ra, 4($sp)
       sw   $a0, 0($sp)
       slti  $t0, $a0, 1
       (a)  $t0, $zero, L1
       addi $v0, $zero, 1
       addi $sp, $sp, (b)
       jr    $ra
L1:    addi $a0, $a0, -1
       (c)  fact
       lw   $a0, (d) ($sp)
       lw   $ra, (e) ($sp)
       addi $sp, $sp, 8
       mul  $v0, $a0, $v0
       jr    $ra
```

Please fill the results in the bank (a), (b), (c), (d), and(e).**(20.points)**

18. According above recursive C language statement, the corresponding ARM assembly code is as:

```
fact:
       SUB    sp, sp #8
       STR    lr, [sp, #4]
       STR    r0, [sp, #0]
       CMP    r0, #1
       (a)    L1
```

```
        MOV   r0,#1
        ADD   sp,sp, #8
        MOV   pc, lr
L1:     SUB   r0, r0, #1
        _(b)_    fact
        MOV   r12, r0
        LDR   r0, [sp, _(c)_]
        LDR   lr, [sp, _(d)_]
        ADD   sp, sp, #8
        MUL   r0, r0, r12
        MOV   _(e)_, lr
```

Please fill the results in the bank (a), (b), (c), (d), and(e).**(20.points)**

19. In the following problems, the data table contains the values for registers r3 and r4. You will be asked to perform several ARM logical operations on these registers.

a. r3 = 0xAAAAAAAA, r4 = 0x12345678

b. r3 = 0xBEADFEED, r4 = 0xDEADFADE

(1). For the lines above, what is the value of r5 for the following sequence of instruction: **(10.points)**

```
ORR r5, r4, r3, LSL #4
```

(2). For the lines above, what is the value of r5 for the following sequence of instructions:(**10.points)**

```
MVN r3, #1
AND r5, r3, r4, LSL #4
```

(3). For the lines above, what is the value of r5 for the following sequence of instructions:(**10.points)**

```
MOV r5, 0xFFEF
AND r5, r5, r3, LSR #3
```

20. The following problems explore number conversions from signed and unsigned binary number to decimal numbers.

a. $1110\ 0110\ 1010\ 1111\ 1111\ 0000\ 0000\ 0010_{two}$

b. $1111\ 1111\ 1111\ 1101\ 1011\ 0011\ 0111\ 0011_{two}$

(1). For the patterns above, what base 10 number does it represent, assuming that it is a two's complement integer?**(10.points)**

(2). For the patterns above, what hexadecimal number does it represent?**(10.points)**

21. The following problems deal with translating from C to **MIPS**. Assume that the variables f, g, h, I and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively.

a. f = g + h +B[4];

b. f = g – A[B[4]];

For the C statements above, what is the corresponding **MIPS** assembly code? **(20.points)**

(You must write the comment after each assembly code, otherwise you won't get any point)

Chapter Exam

Chapter 3 Arithmetic for Computers

2011/05/03

22. Assume A and B in the following table are signed 8-bit decimal integers stored in sign-magnitude format. (1) Calculate A+B. (2) Is there overflow, underflow, or neither? **(20 Points)**

A	B
69	90

23. Let's look in more detail at multiplication. We will use the numbers in the following table.

A	B
$101000_{(2)}$	$010011_{(2)}$

Using the hardware described in Figure 1 to calculate the product of two unsigned 6-bits binary numbers A and B. Complete the contents of each register on each step list on the following table. **(60 Points)**

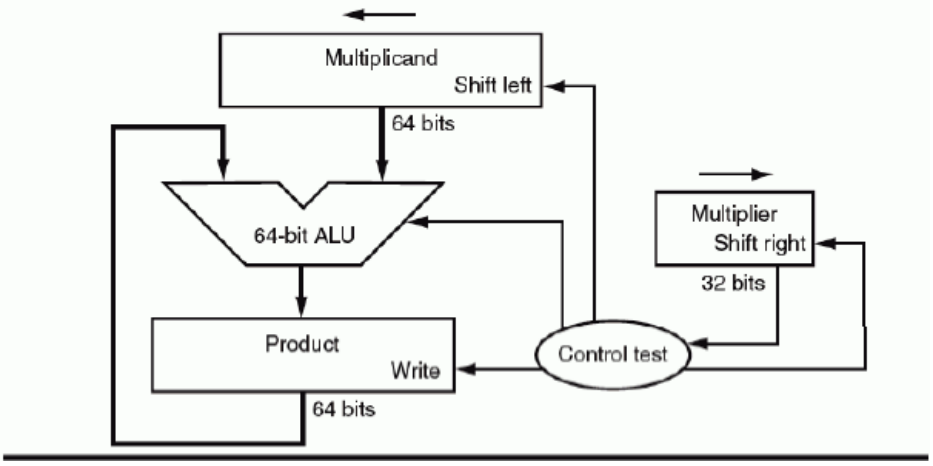

Figure 1 First version of the multiplication hardware

Step	Action	Multiplier	Multiplicand	Product
0	Initial values	010 011	000 000 101 000	000 000 000 000
1	Prod = Prod + Mcand			
	Lshift Mcand			
	Rshift Mplier	(1)	(6)	(11)
2	Prod = Prod + Mcand			
	Lshift Mcand			
	Rshift Mplier	(2)	(7)	(12)

3	LSB = 0			
	Lshift Mcand			
	Rshift Mplier	(3)	(8)	(13)
4	LSB = 0			
	Lshift Mcand			
	Rshift Mplier	(4)	(9)	(14)
5	Prod = Prod + Mcand			
	Lshift Mcand			
	Rshift Mplier	(5)	(10)	(15)
6	LSB = 0			
	Lshift Mcand			
	Rshift Mplier	000 000	101 000 000 000	001 011 111 000

24. What decimal number does the following bit pattern represent: **0x24A60000**? If it is a floating-point number using the IEEE 754 standard. **(20 Points)**