Electronics Ph. D. Qualification Exam. 2021 [calculator allowed, but not mobile phone] 01/20/2021

Name: ID#

Useful CMOS parameters and equations, Diode current $I_D = I_S \exp\frac{V_F}{V_T}$

$\mu_n C_{ox} = 200\mu A/V^2$, $\mu_p C_{ox} = 100\mu A/V^2$, $V_{THN} = 0.4$, $V_{THP} = -0.4$, $r_o = 1/\lambda I_D$

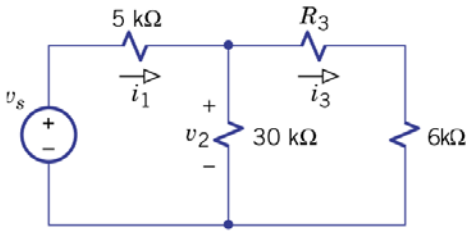
$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})^2\right]$ [Transistor operated at saturation region, $V_{GS}-V_{TH} > 0$ and $V_{DS} > V_{GS}-V_{TH}$]

$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{\mu_n C_{ox}\frac{W}{L} I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$ [Transconductance]

$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})\right]}$ [Transistor on Resistance]

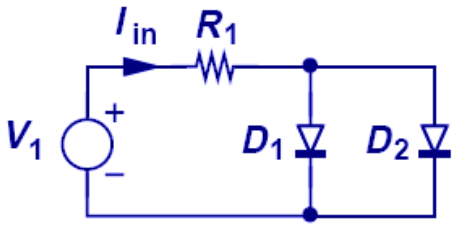
$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{\mu_n C_{ox}\frac{W}{L} I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$ [Transconductance]

1. If the circuit in the following figure represents a source and load with v_s=75V, and R_3=54 kΩ , then **what are the values of (a) i_1 and (b) i_3** ? (5%)

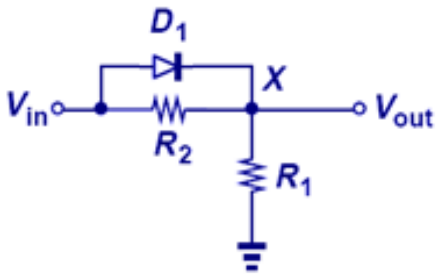


2. Consider a *pn* junctions in forward bias. Initially a current of 5 mA flows through it, and the current increases by 8 times hen the forward voltage is increased by 1.5 times. Determine the initial bias applied and reverse saturation current. (V_T = 26mV) (5%)

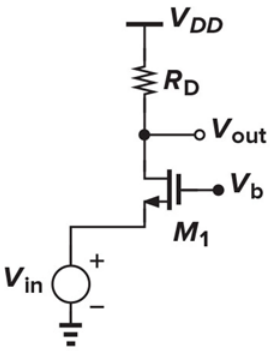
3. D_1 and D_2 have different cross section areas but are otherwise identical. Determine the current flowing through each diode in terms of I_{in}, I_{S1}, and I_{S2}. (5%)



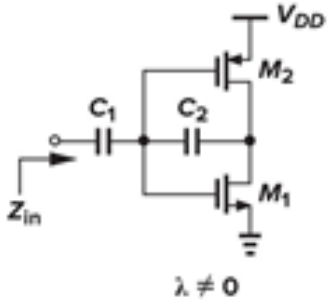
4. Plot the input/output characteristic of the following circuit using the constant voltage model ($V_{D,on}$). (5%)



5. A Common Gate stage with a RG in series of gate of MOS including C_{GS} and C_{GD} only, please find the transfer function V_{out}/V_{in}. assume $\lambda=\gamma=0$. (10%)



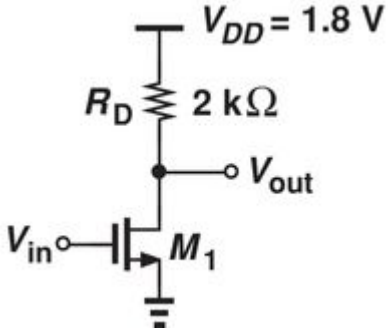
6. Please find input impedance of the following circuits, ignoring all other capacitances. (10%)



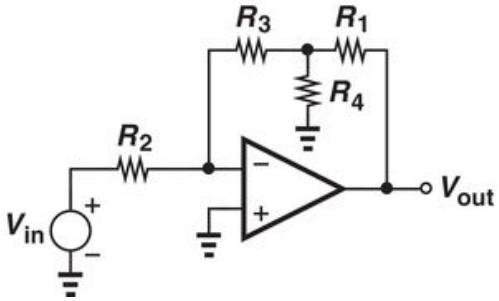
7. An NMOS device carries 1 mA with $V_{GS} - V_{TH}$ = 0.6 V and 1.6 mA with $V_{GS} - V_{TH}$ = 0.8 V. If the device operates in the triode region, calculate V_{DS} and W/L. (10%)

Ans:

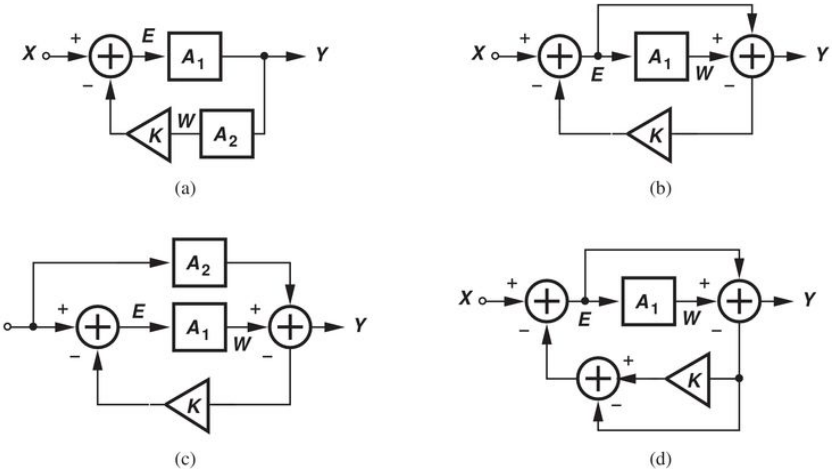
8. In the common-source stage shown below, W/L = 30/0.18 and $\lambda = 0$. (a) What gate voltage yields a drain current of 0.5 mA? (Verify that M_1 operates in saturation.) (b) With such a drain bias current, calculate the voltage gain of the stage. (10%)



9. Assuming $A_0 = \infty$, compute the closed loop gain of the inverting amplifier shown below. Verify that the result reduces to expected values if $R_1 \to 0$ or $R_3 \to 0$. (12%)



10. Determine the transfer function. Y/X, for systems shown below. (12%)



11. For each NMOS section shown below, draw the dual PMOS section, construct the overall CMOS gate, and determine the logical function performed by the gate. (16%)