國立中山大學 103 學年度第一學期資工系數位系統期末考試

學號：　　姓名：

一、選擇與是非題（每題 3 分，12 分）

(　　) 1. What kind of flip-flop is the most popular component to construct a register? ①*SR* ②*D* ③*JK* ④*T*

(　　) 2. How many address lines are required in a 16M×16 RAM? ①14 ②16 ③24 ④34.

(　　) 3. In DRAM, information is stored in the form of charges on capacitors. When compared to SRAM, DRAM has shorter read/write cycle.

(　　) 4. Programmable read-only memory (PROM) has programmable AND array and fixed OR array.

二、問答題（88 分）

1. Derive the following terms for the sequential circuit shown in Fig. 1.
(1) Input (Excitation) equations (6%)　(2) State equations and output equation (6%)
(3) State table (Table 1) (6%)　(4) State diagram (4%)

2. Design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6. Assume that binary states 011, 101 and 111 are considered as don't care conditions.
(1) Complete the state table as shown in Table 2 using natural binary encoding for state assignment. (4%)
(2) Use D flip-flops and derive the simplified flip-flop input (excitation) equations using the K-map (find the minimal sum of products expressions). (6%)
(3) Draw the logic diagram of the counter with D flip-flops as shown in Fig. 2(a). (4%)
(4) Use T flip-flops and complete the state table and T flip-flop input as shown in Table 2. (4%)
(5) Use T flip-flops and derive the simplified flip-flop input (excitation) equations using the K-map (find the minimal sum of products expressions). (6%)
(6) Draw the logic diagram of the counter with T flip-flops as shown in Fig. 2(b). (4%)

3. A 64K × 8 memory uses coincident decoding by splitting the internal decoder into *X*-selection and *Y*-selection as shown in Fig. 3.
(1) What is the size of each decoder, and how many AND gates are required for decoding the address? (6%)
(2) Determine the *X* and *Y* selection lines that are enabled when the input address is the binary equivalent of 36,952. (6%)

4. Using an 8 × 3 ROM shown in Fig. 4 and a 3 × 4 × 3 PLA shown in Fig. 5, implement the truth table shown in Table 3. (6%) (10%)

5. Explain the read and write operations of the 4 × 4 RAM and the memory cell as shown in Fig. 6(a) and 6(b), respectively. (10%)

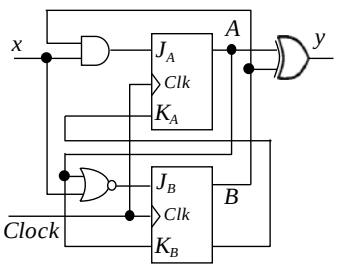

Fig. 1

Table 1

Present state		Input	Next state		Output
A	*B*	*x*	*A*	*B*	*y*

Table 2

Present state			Next state			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}

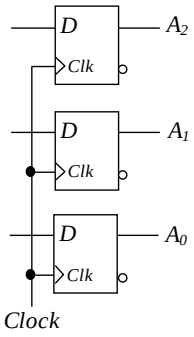

Fig. 2(a)

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Fig. 3

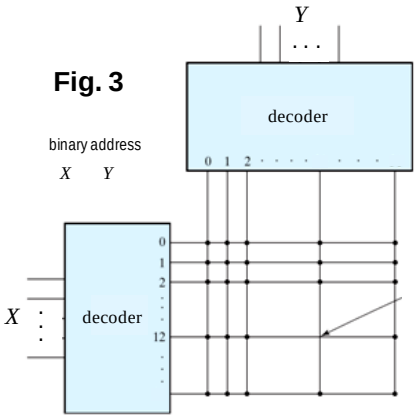

Table 3

A	B	C	F_1	F_2	F_3
0	0	0	1	0	1
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	1	0	1

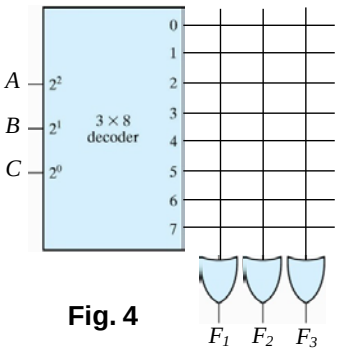

Fig. 4

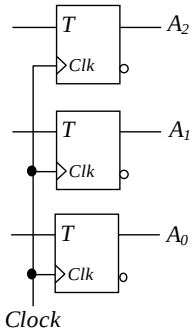

Fig. 2(b)

Fip-flop	D	JK	T
characteristic equation	$Q(t+1) = D$	$Q(t+1) = JQ'+K'Q$	$Q(t+1) = T \oplus Q$

characteristic table

D	Q(t + 1)
0	0
1	1

J	K	Q(t + 1)
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$

T	Q(t + 1)
0	$Q(t)$
1	$Q'(t)$

excitation table

Q(t)	Q(t + 1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q(t)	Q(t + 1)	T
0	0	0
0	1	1
1	0	1
1	1	0

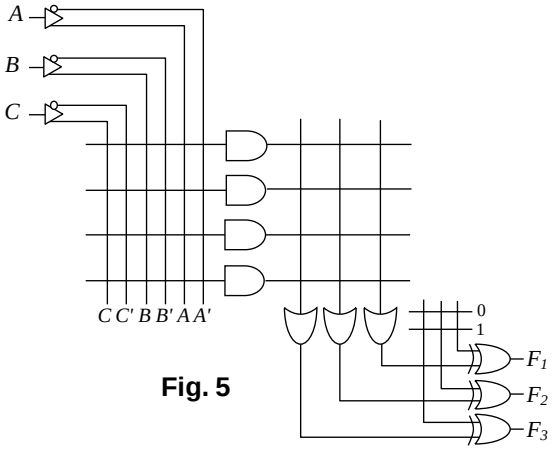

Fig. 5

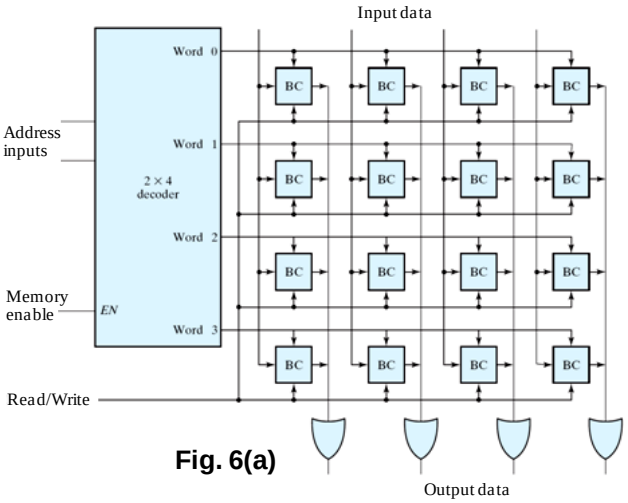

Fig. 6(a)

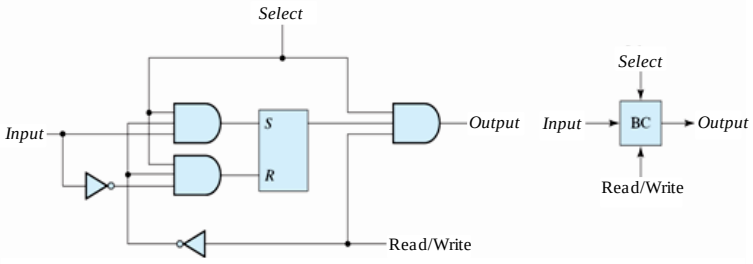

Fig. 6(b)