# 國立中山大學 101 學年度第一學期資工系組合語言與微處理機期中考試題

學號：　　姓名：

一、選擇與是非題（每題 3 分，21 分）

(　　) 1. 下列何者不是精簡指令集電腦(RISC)的特性？ ① fixed instruction size with few formats ② pipelined execution ③ good code density ④ load-store architecture。

(　　) 2. 下列何者不是 ARM architecture 的特性？ ① conditional execution of every instruction ② a load-store architecture ③ 3-address instructions ④ single-cycle execution of all instructions。

(　　) 3. 下列那一個指令不會設定 conditional codes？①MOVS ②SBC ③CMP ④TST。

(　　) 4. 撰寫 ARM 的 user-level program 時，不會用到下列哪一個 register？ ① r0～r14 ② r15 ③ SPSR (Saved program status register) ④ CPSR (current program status register)。

(　　) 5. 在 5-stage pipeline ARM organization 中的 forwarding paths 可以直接將 ALU 或是 Data cache 的輸出值在下一個 clock cycle 直接傳送至 ①Register bank ②ALU 的輸入③Data cache ④以上皆是。

(　　) 6. 執行 ASR 指令時，左邊（the most significant end）空出的位元會被填入 zeros。

(　　) 7. Multiple register transfer addressing modes 中的 STMIA 與 STMEA 指令代表相同的意義。

二、問答題（82 分）

**1.** Fill the following output controls signals used in MU0 (Fig. 1). The enable signal like ACCce, PCce is active high. If RnW equals 1, the memory will be read. (10%)

| Inputs | | | | | | Outputs | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Instruction | Opcode | Reset | Ex/ft | ACCz | ACC15 | Asel | Bsel | ACCce | PCce | IRce | ACCoe | ALUfs | MEMrq | RnW | Ex/ft |
| LDA S | 0000 | 0 | 0 | x | x | | | | | | 0 | =B | | | 1 |
| | 0000 | 0 | 1 | x | x | 0 | 0 | 0 | 1 | 1 | 0 | B+1 | 1 | 1 | 0 |
| ADD S | 0010 | 0 | 0 | x | x | | | | | | 0 | A+B | | | 1 |
| | 0010 | 0 | 1 | x | x | 0 | 0 | 0 | 1 | 1 | 0 | B+1 | 1 | 1 | 0 |
| JMP S | 0100 | 0 | x | x | x | | | | | | 0 | B+1 | | | 0 |

**2.** What is the addressing mode? Explain the following addressing modes and write down an ARM instruction with the addressing mode: Immediate addressing, Base plus offset addressing, and Base plus scaled index addressing. (8%)

**3.** Please explain the meaning of the following ARM instructions. (16%)

(1) ADD r0, r0, r0, LSL #1
RSB r0, r0, r0, LSL #3

(2) ADDS r2, r2, r0
ADC r3, r3, r1

(3) LDR r0, [r1], #4
STMFD r13!, {r2-r9}

(4) CMP r0, #3
ADDNE r1, r1, r0

**4.** Find out if the following instruction format is correct or not. If incorrect, point out the problem. (16%)

(1) LDMFB r1!, {r5, r4, r9}

(2) ADD r3, r5, #1023

(3) MOVS r4, r4, RRX #2

(4) SUB r1, r2, r3, LSL #32

**5.** Please indicate the datapath activities for the different type of instructions in Fig. 2. (10%)

**6.** For the following C-expression: if((r0==r1) && (r2==r3)) r4++;

(1) Write down the corresponding ARM code without using the conditional execution. (But you can still use conditional branches.) (6%)

(2) Write down the corresponding ARM code using the minimum number of instructions. (6%)

**7.** Please briefly explain the type of ARM exceptions, and ARM architecture how to handle an exception (including exception entry and exception return). (10%)

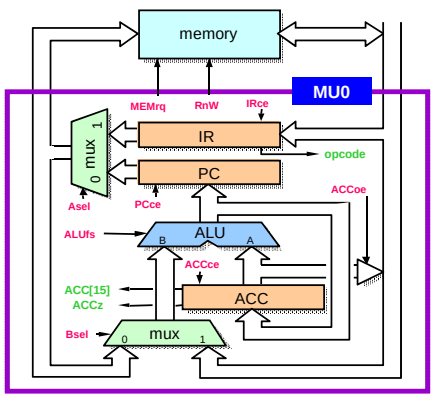
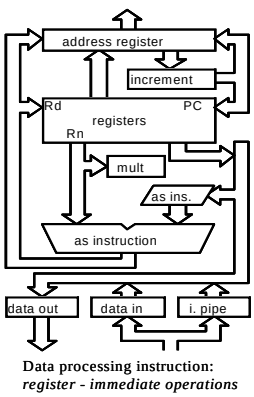
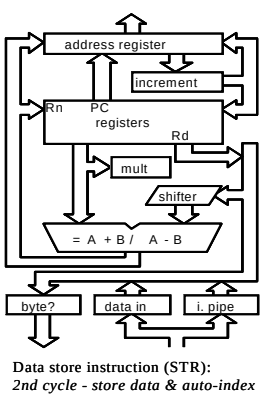



Fig. 1




Data processing instruction:
*register - immediate operations*

Fig. 2(a)




Data store instruction (STR):
*2nd cycle - store data & auto-index*

Fig. 2(b)