國立中山大學 101 學年度第一學期資工系數位系統期末考試

學號：　　姓名：

一、選擇與是非題（每題 3 分，12 分）

(　　) 1. How many address lines are required in a 64M×16 RAM? ①16 ②26 ③30 ④64

(　　) 2. The master-slave D flip-flop shown in Fig. 1(a) is a positive-edge-triggered flip-flop.

(　　) 3. The outputs of a Moore state machine are functions of both the present state and inputs.

(　　) 4. Programmable ROM has a programmable AND array and a fixed OR array.

二、問答題（94 分）

1. Please answer the following problems.
(1) Fig. 1(a) shows a master-slave D flip-flop. Complete the timing diagram shown in Fig. 1(b). (6%)
(2) Briefly explain the operations of the 4-bit up/down binary counter shown in Fig. 2. (6%)

2. The state diagram for sequence detector which detects a sequence of two or more consecutive 1's in a string of bits coming through an input line *x* is shown in Fig. 3(a).
(1) Complete the state table as shown in Table 1 using natural binary encoding for state assignment (i.e., S_0 = 00, S_1 = 01, S_2 = 10). (5%)
(2) Use D flip-flops and derive the simplified flip-flop input (excitation) equations and output equation using the K-map. (4%)
(3) Draw the logic diagram of sequence detector with D flip-flops as shown in Fig. 3(b). (4%)
(4) Use JK flip-flops and complete the state table and JK flip-flop input as shown in Table 2. (6%)
(5) Use JK flip-flops and derive the simplified flip-flop input (excitation) equations using the K-map. (6%)
(6) Draw the logic diagram of sequence detector with JK flip-flops as shown in Fig. 3(c). (4%)

3. Design a serial adder using a JK flip-flop as shown in Fig. 4.
(1) Complete the state table as shown in Table 3. (8%)
(2) Derive the simplified flip-flop input (excitation) equations. (6%)
(3) Draw the logic diagram with a JK flip-flop as shown in Fig. 4. (5%)

4. Design the synchronous sequential circuit using T flip-flops with the state diagram as shown in Fig. 5(a).
(1) Complete the state table as shown in Table 4. (8%)
(2) Derive the simplified flip-flop input (excitation) equations. (6%)
(3) Draw the logic diagram with T flip-flops as shown in Fig. 5(b). (5%)

5. Using an 8 × 2 ROM shown in Fig. 6 and a 3 × 4 × 2 PLA shown in Fig. 7, implement the truth table shown in Table 5. (15%)

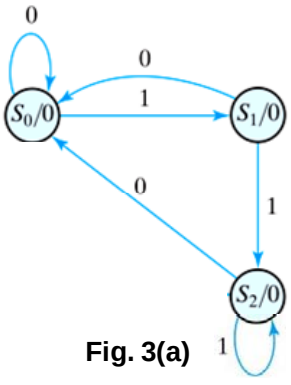

Fig. 3(a)

Table 1

Present State A	Present State B	Input x	Next State A	Next State B	Output y
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Table 2

Present State A	Present State B	Input x	Next State A	Next State B	Flip-Flop Inputs J_A	K_A	J_B	K_B
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

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Fip-flop	D	JK	T
characteristic equation	$Q(t+1) = D$	$Q(t+1) = JQ' + K'Q$	$Q(t+1) = T \oplus Q$

characteristic table

D	Q(t + 1)
0	0
1	1

J	K	Q(t + 1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q′(t)

T	Q(t + 1)
0	Q(t)
1	Q′(t)

excitation table

Q(t)	Q(t + 1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q(t)	Q(t + 1)	T
0	0	0
0	1	1
1	0	1
1	1	0

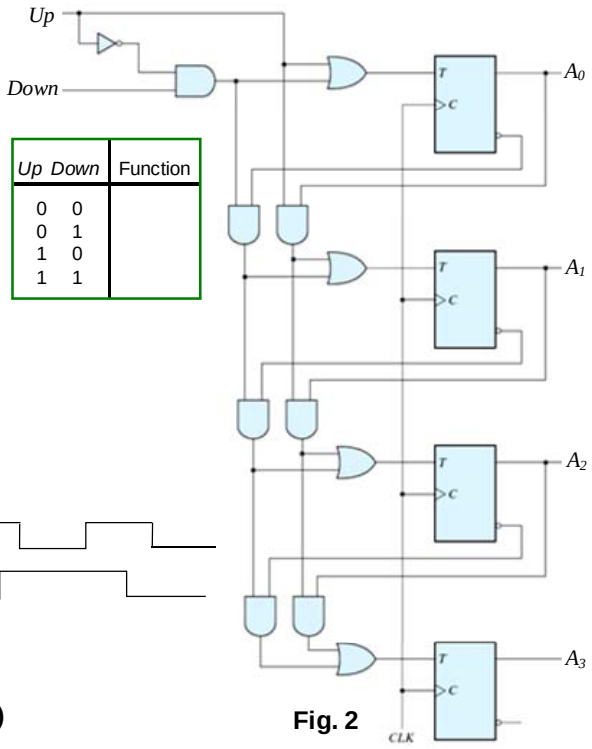

Fig. 2

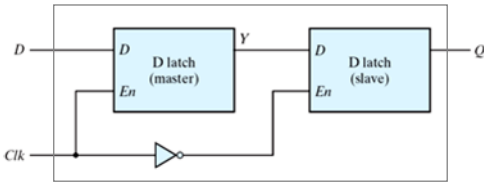

Fig. 1(a)

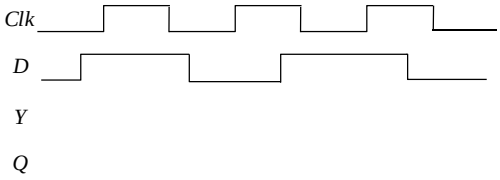

Fig. 1(b)

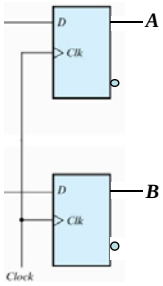

Fig. 3(b)

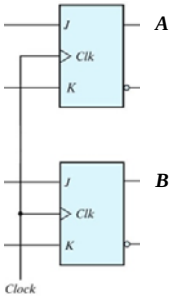

Fig. 3(c)

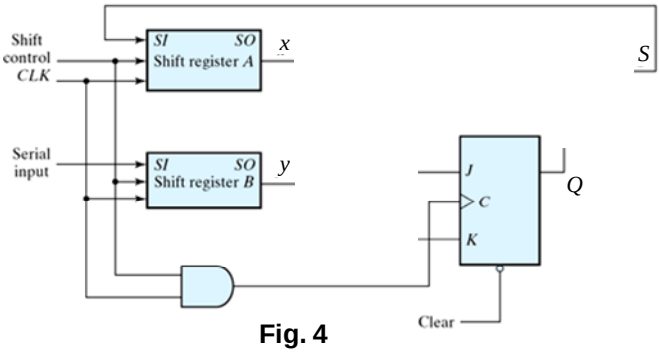

Fig. 4

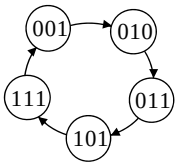

Fig. 5(a)

Table 4

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}

Table 3

Present State	Inputs		Next State	Output	Flip-Flop Inputs	
Q	x	y	Q	S	J_Q	K_Q
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

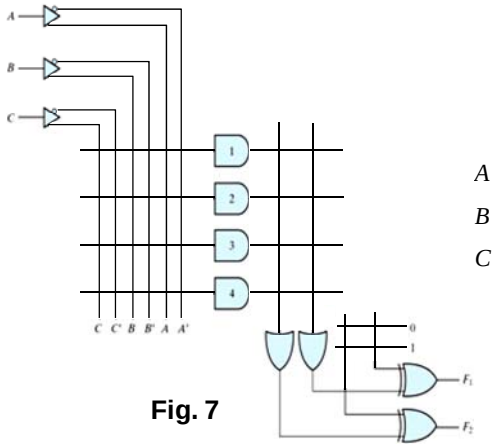

Fig. 7

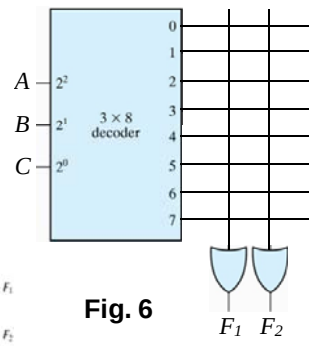

Fig. 6

Table 5

A	B	C	F_1	F_2
0	0	0	1	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

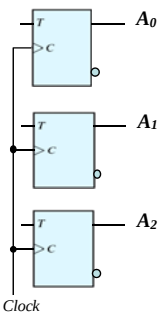

Fig. 5(b)