國立中山大學一百學年度第一學期資工系數位系統期中考試

學號：　　姓名：

一、選擇與是非題（每題 3 分，15 分）

(　　) 1. 下列何者錯誤？① product of maxterms is canonical form ② $F(x, y, z) = y' + zy + x'yz'$ is standard form ③ $F(w, x, y, z) = wx + y(z+w)$ is standard form ④ combinational circuits 中沒有 feedback path。

(　　) 2. 下列那一個 two-level form 是 degenerate form (亦即可轉換成 a single operation)？① NOR-OR ② NAND-NAND ③ OR-NAND ④ NAND-OR。

(　　) 3. 關於 XOR 以及 XNOR，何者錯誤？ ① $(x \oplus y)' = x \odot y$ ② $x \oplus y' = (y \oplus x)'$ ③ $x \oplus 1 = x'$ ④ $x \oplus x' = 0$。

(　　) 4. 一般而言，Product of sums 應該轉換成 NAND Implementation，而 Sum of products 則應該轉換成 NOR Implementation 以獲得較簡單的電路。

(　　) 5. 對於 three-bit message x, y, z 而言，假如 parity bit $P = x \oplus y \oplus z$ 且 parity check $C = x \oplus y \oplus z \oplus P$，則 P 為 odd parity bit 且 $C = 0$ 代表沒有發生錯誤或是 x、y、z、P 中有偶數個位元發生錯誤。

二、問答題（85 分）

1. (1) Find the signed-magnitude and two's complement representations of the decimal number: –98　(4%)
(2) Use De Morgan's law to derive the complement of the following Boolean function:　$F(x, y, z) = x + y(x'+xz)$,　$F' = ?$　(4%)

2. (1) Derive the sum-of-minterms and the product-of-maxterms canonical forms for Boolean function $F(w, x, y, z) = (x+z')(x'+y+z)(w'+x+y'+z')$.　(8%)
(2) Using the Karnaugh map to find the simplest sum-of-products and product-of-sums of this Boolean function.　(10%)
(3) Implement the function $F(w, x, y, z)$ with NAND-NAND and NOR-NOR logics, draw the logic diagrams.　(8%)

3. Using the Karnaugh map to find all the simplest sum-of-products of Boolean function $F(v, w, x, y, z) = \sum m(0, 1, 2, 3, 8, 9, 10, 11, 13, 15, 16, 17, 18, 19, 24, 26, 29, 31)$.　(8%)

4. Design a code converter that can convert the BCD code *ABCD* to excess-3 code *wxyz*.
(1) Derive the truth table　(3%)
(2) Derive the simplified Boolean functions　(8%)
(3) Draw the logic diagram　(3%)

5. List the truth table, derive the simplified Boolean functions, and draw the logic diagrams of the following circuits with XOR function.
(1) The half adder (inputs: *x*, *y* and outputs: *C*, *S*) with XOR gate.　(4%)
(2) The full adder (inputs: *x*, *y*, *z* and outputs: *C*, *S*) with two half adders and an OR gate.　(6%)

6. Design a 4-bit adder with inputs $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$, and outputs $S = S_3S_2S_1S_0$ and C_4.
(1) Draw the block diagram of 4-bit ripple-carry adder.　(3%)
(2) Let carry propagate $P_i = A_i \oplus B_i$ and carry generate $G_i = A_iB_i$, then sum $S_i = P_i \oplus C_i$ and carry $C_{i+1} = G_i + P_iC_i$, where $0 \le i \le 3$. Derive the Boolean functions of C_1, C_2, C_3, and C_4. Draw the carry lookahead generator.　(12%)
(3) Draw the 4-bit carry lookahead adder with carry lookahead generator. (4%)