計算機結構資格考

1. (20%)

The dynamic power (active power) is in general proportional to 1/2 * capacitive load * voltage^2 * frequency switched. On the other hand, the static power (leakage power) is usually independent of the working frequency. Processor A, fabricated using a process technology, has a clock rate of 3.6 GHz and voltage of 1.25 volts. Assume that, on average, it consumed 10W of static power and 90 W of dynamic power. Processor B, fabricated with a more advanced process technology, has a clock rate of 3.4 GHz and voltage of 0.9 volts. Assume that, on average, it consumes 30W of static power and 40 W of dynamic power.

1.1 **(5%)** What is the total energy (in unit of joules) consumed if a task is run on processor A with total execution time of 100 seconds.

1.2 **(5%)** If the same task is run on a slower version of processor A with half working frequency of 1.8 GHz, assuming the static power is unchanged and the total execution time is two times larger, what is the total energy consumed?

1.3 **(5%)** For each processor, find the total capacitive load.

1.4 **(5%)** For each process technology, find the percentage of the total dissipated power comprised by the static power, i.e., the ratio of static power to total power.

2. (20%)

Briefly answer the follow questions.

2.1 **(5%)** What is branch history table (BHT)? Explain how to use BHT to speed up the execution of branch instructions.

2.2 **(5%)** What is branch target buffer (BTB)? Explain how to use BTB to speed up the execution of branch instructions.

2.3 **(5%)** What is two-level (correlation) branch prediction? Explain how it works.

2.4 **(5%)** Do Intel's Core i7 CPU and AMD's Opteron CPU have the same instruction set architecture (ISA)? Do ARM's Cortex A-9 and ARM's Cortex A-15 have the same ISA?

3. (15%) Performance Calculation

3.1 **(5%)** Suppose our processor is an ideal 5-stage pipeline with separate instruction cache (I-cache) and data cache (D-cache). The CPI_{ideal} is 1 clock cycle, whereas memory access takes 200 cycles. The miss rate of I-cache and D-cache miss rate is 5%. Assume that 50% of our instructions are loads or stores. What is our processor's CPI_{stall} if considering the stalls due to cache miss?

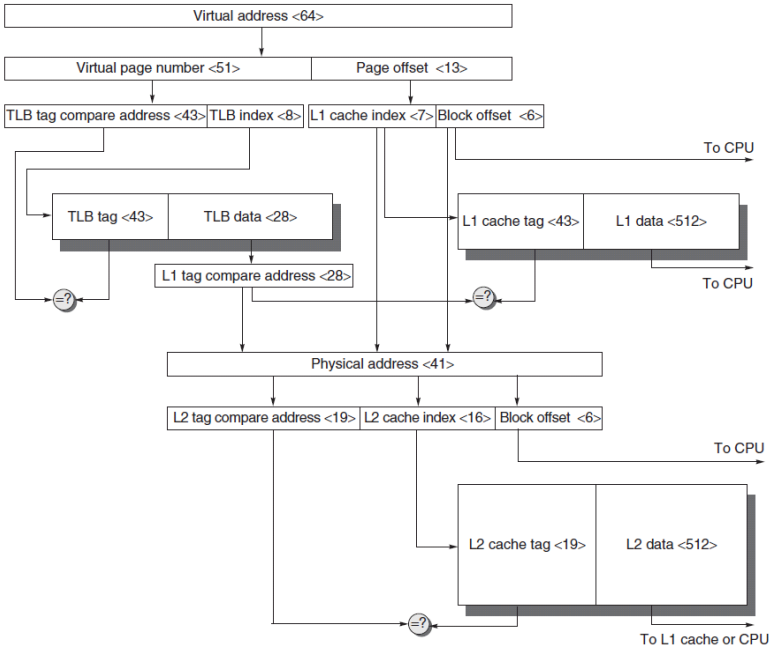
3.2 **(5%)** To improve the performance of our processor, we add a unified L2 cache between the

two L1 caches and main memory. Our L2 cache has a hit time of 20 cycles and a *global* miss rate of 3%. What is our new CPI_{stall}? What is the local miss rate of L2 cache?

3.3 **(5%)** If we try to further improve the performance by adding a unified L3 cache with L3 cache hit time of 40 cycles and a *local* miss rate of 50%. What is our new CPI_{stall}?

4. (20%) Memory Hierarchy

The following figure shows a hypothetical memory hierarchy where all the caches are direct-mapped.



4.1 **(5%)** What is the size of L1 cache? What is the block size of L1 cache? What is the page size?

4.2 **(5%)** What is the number of entries in the TLB? What is the information stored in the TLB tag field? What is the information stored in the TLB data field?

4.3 **(5%)** What is the size of L2 cache? What is the block size of L2 cache?

4.4 **(5%)** What are the advantages of virtual-addressed physical-tagged cache? Is this cache system virtual-addressed physical-tagged cache?

5. (25%)

5.1 (5%) What is the advantage of single instruction multiple data (SIMD)? Compare the differences between SIMD in conventional CPU (Central Processing Units) and SIMD in GPU (Graphics Processing Units)

5.2 (5%) Give examples to explain the differences of spatial locality and temporal locality during execution of a computation task in CPU.

5.3 (5%) What is static multiple issue? What is dynamic multiple issue? Compare the differences?

5.4 (5%) Consider the following MIPS loop. Assume that register $t1 is initialized to the value of 10. What is the value in register $s2 assuming $s2 is initially zero?

```
LOOP:   slt $t2, $0, $t1       # set $t2=1 if 0 < $t1
        beq $t2, $0, DONE
        add $s2, $s2, $t1    # $s2 = $s2 + $t1
        subi $t1, $t1, 1       # $t1 = $t1 - 1
        j      LOOP
DONE:
```

5.5 (5%) Assume the base addresses of two arrays x[i] and y[i] are in registers $s1 and $s2 respectively, and the initial value of the variable z is in the floating-point register pair $f8/$f9. What are the corresponding C statements of the following MIPS assembly code segment?

```
        li $s5, 32      #load immediate value, $s5=32
        li $s0, 0
L:      sll $s4, $s0, 3
        addu $t1, $s1, $s4
        addu $t2, $s2, $s4
        l.d $f2, 0($t1)
        l.d $f4, 0($t2)
        mul.d $f6, $f2, $f4
        add.d $f8, $f6, $f8
        addi $s0, 1
        bne $s0, $s5, L
```