Department of Computer Science and Engineering
National Sun Yat-sen University
First Semester of 2022 PhD Qualifying Exam

Subject： Computer Architecture

Problem 1: (15 points)

Figure 1 shows a 5-stage pipelined MIPS CPU to support a simple code in Figure 2. We need to spend one clock cycle to complete all tasks in each pipeline stage.

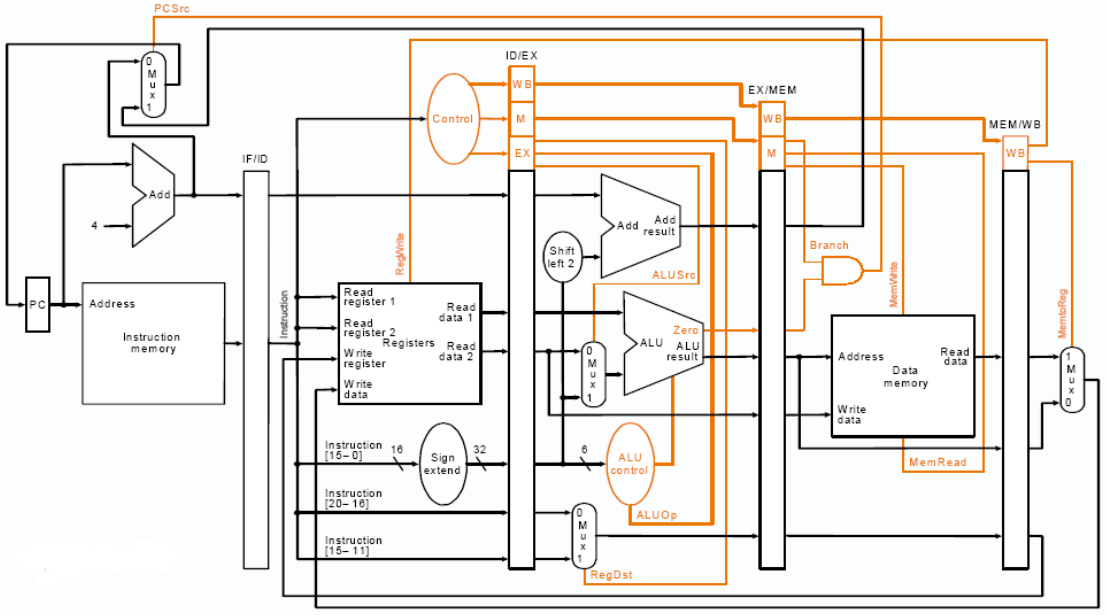

Figure 1

```
sub   $2, $1, $3
and   $12, $2, $5
or    $13, $6, $2
add   $14, $2, $2
sw    $15, 100($2)
```

Figure 2

1. (5%) Do we need to stall this architecture in Figure 1 to run the code in Figure 2? If yes, please determine how many cycles we should stall and explain your reasons. If not, please describe your reason.
2. (5%) To support the code in Figure, please design a minimum viable product (MVP) of the ALU in Figure 1. You need to show the ALU architecture.
3. (5%) Is it possible to move the Adder from the third pipeline stage to the second pipeline stage? If yes, please explain your re-design strategy. If not, please describe your reason.

Problem 2: (30 points)

You have to run a program, which requires 4GB of memory space. Unfortunately, your computer system only allocates 2GB DRAM to this program. Hence, it is necessary to apply the virtual memory technique, and we assume that the total page size is 4KB. Besides, you implement the write-back consistency policy and the LRU replacement policy in this virtual memory technique as well.

1. (10%) How large is the involved page table at least?
2. (10%) We assume that the CPU in your system access the data in this program randomly (i.e., no data locality). At the quasi-stationary, please show the approximated page fault rate.
3. (10%) If we have a TLB in this system and the TLB miss rate is 75% at the quasi-stationary, how large is the involved TLB at least?

Problem 3: (25 points)

Now, you have a 32-bit processor, which includes a cache with 16KB data. We assume that the write-back consistency policy and the LRU replacement policy are both implemented in this cache as well. Please analyze the different architecture designs below.

1. (5%) How many total bits are required if the direct-mapping strategy is involved, and the one-word block is considered?
2. (5%) How many total bits are required if the direct-mapping strategy is involved, and the four-word block is considered?
3. (5%) How many total bits are required if the two-way set-associative strategy is involved, and the four-word block is considered?
4. (5%) TLB is usually adopted in modern systems. If we use the 32-bit address to access the TLB and each page size is 4KB, how large is the involved TLB?
5. (5%) By following the previous question, how large is the involved page table?

Problem 4: (30 points)

You have to run a program, which requires 4GB of memory space. Unfortunately, your computer system only allocates 2GB DRAM to this program. Hence, it is necessary to apply the virtual memory technique, and we assume that the total page size is 4KB. Besides, you implement the write-back consistency policy and the LRU replacement policy in this virtual memory technique as well.

1. (10%) How large is the involved page table at least?
2. (10%) We assume that the CPU in your system access the data in this program randomly (i.e., no data locality). At the quasi-stationary, please show the approximated page fault rate.
3. (10%) If we have a TLB in this system and the TLB miss rate is 75% at the quasi-stationary, how large is the involved TLB at least?