Signal Integrity of IC, package and PCB co-design

智原科技

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(Technical Director)
2011/10/07

FARADAY

Agenda

- **Introduction**
  - Faraday profile
  - Market position
  - Core competence
- **System Signal Integrity**
- **Case Studies**
- **Summary**

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Faraday At A Glance

2010

- Achieved yearly revenue breakthrough of US$200 millions
- More than 20% shipment comes from SoC design
- Around 700 employees worldwide, 500+ in R&D

2006-2009

- The shipment of USB 2.0 achieved 200 millions, announced other HSIO of SATA2, PCIe2, MIPI, DDR3
- License ARM v5 architecture

2000-2005

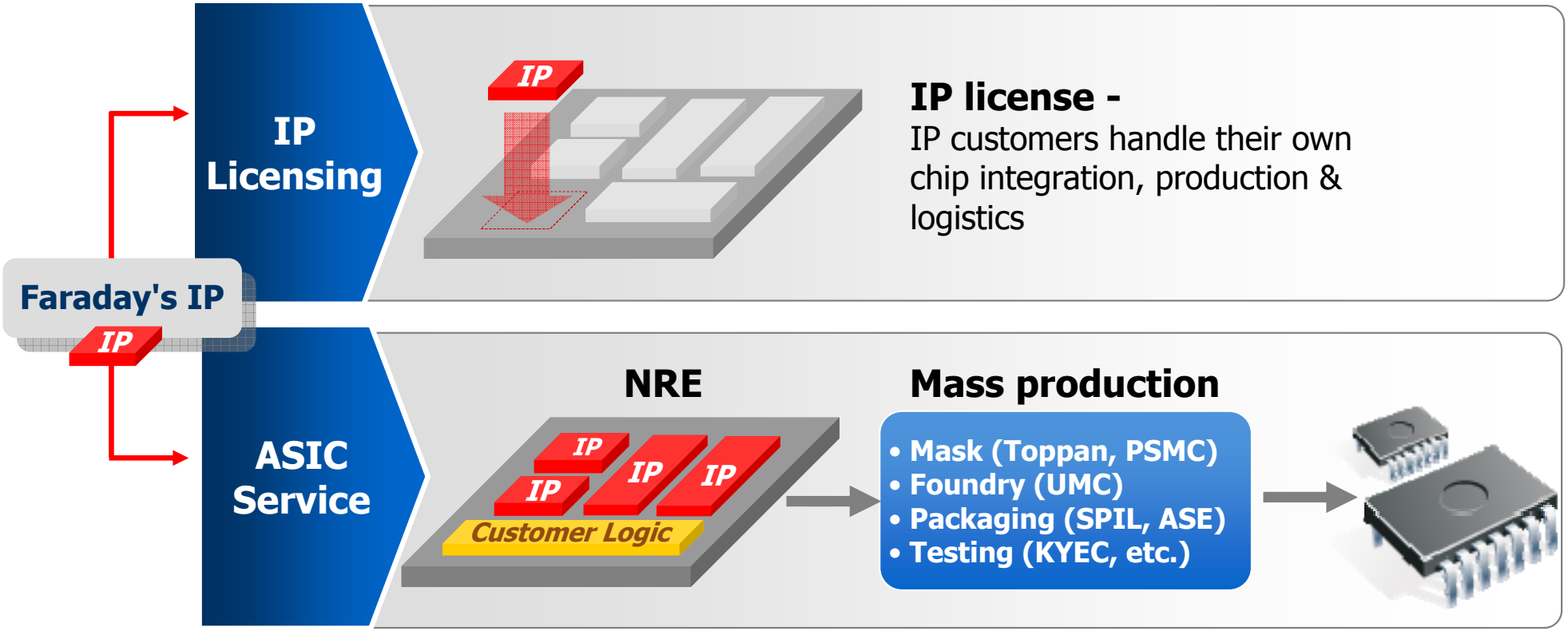
- Achieved yearly revenue breakthrough of US$100 millions
- Awarded with "Design Company with the Most Potential" by Business Weekly Magazine

1993-1999

- 1999: Listed in Taiwan Exchange (TAIEX:3035)
- 1993: Founded as the first fabless ASIC design service provider in ASIA

Faraday Global Presence

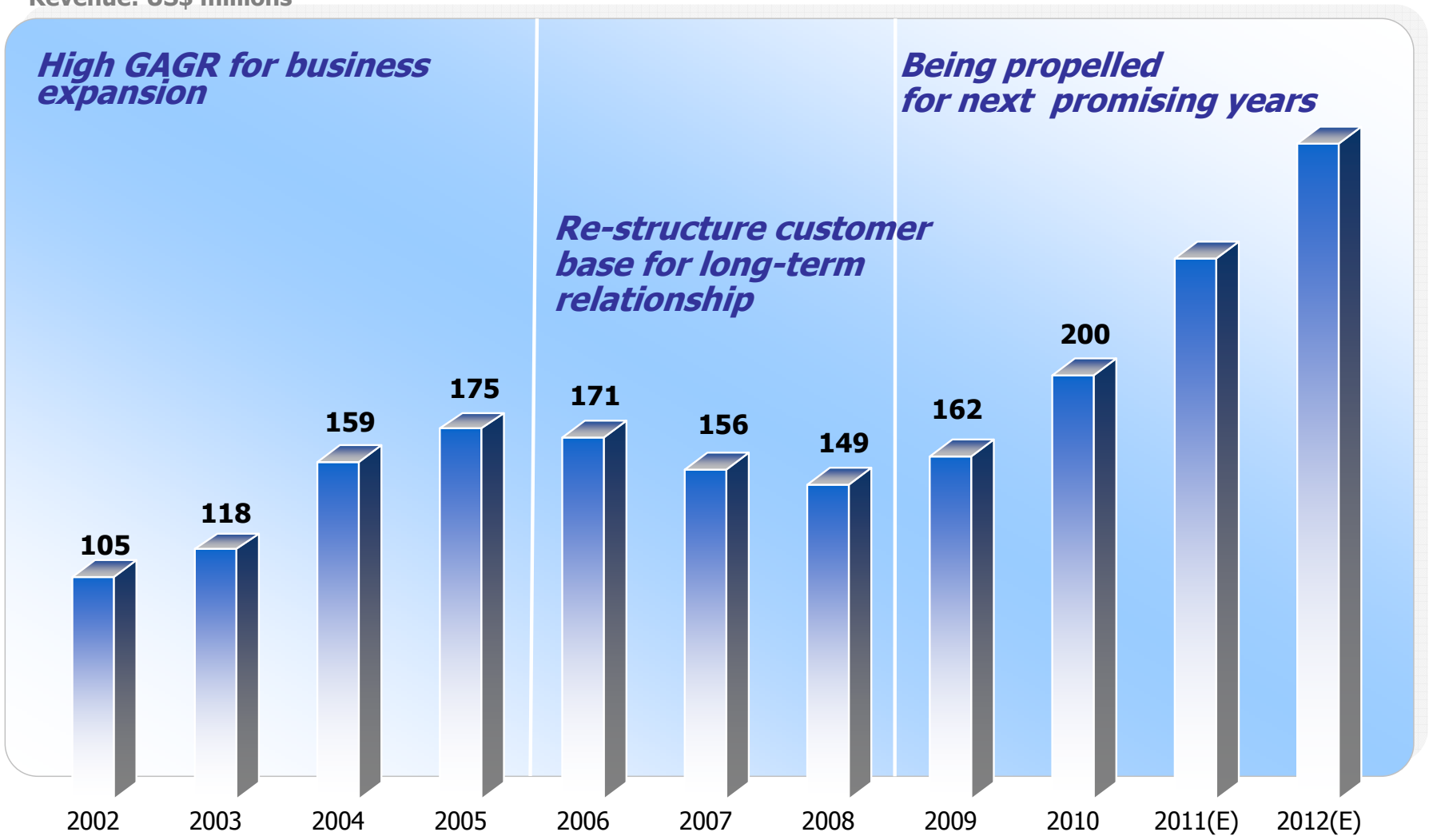
Business Model



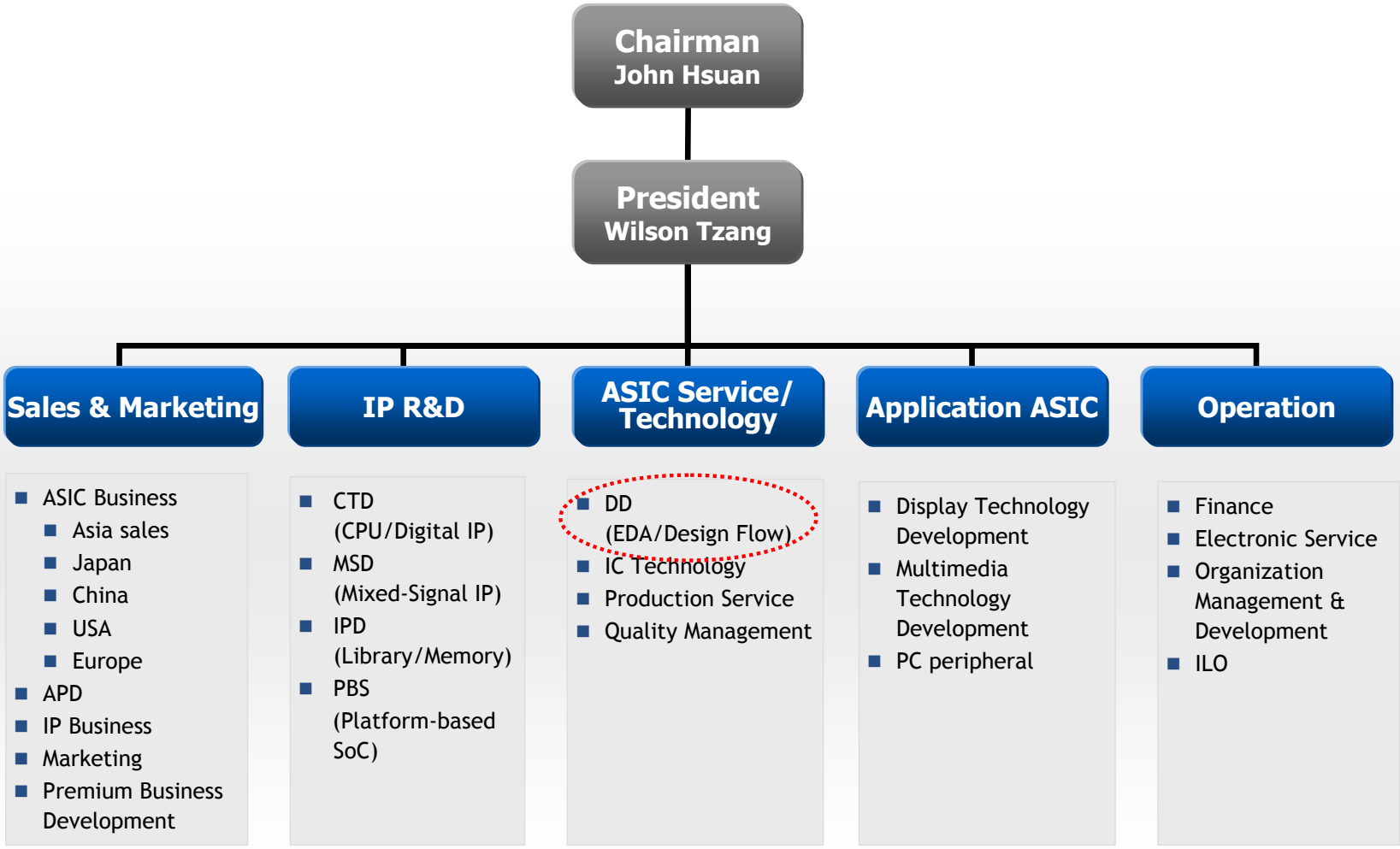
- **Business leverage**
  - In-house IP pool to shorten time for integration & minimize the risk
  - ASIC experiences to maximize the IP value

Revenue Chart

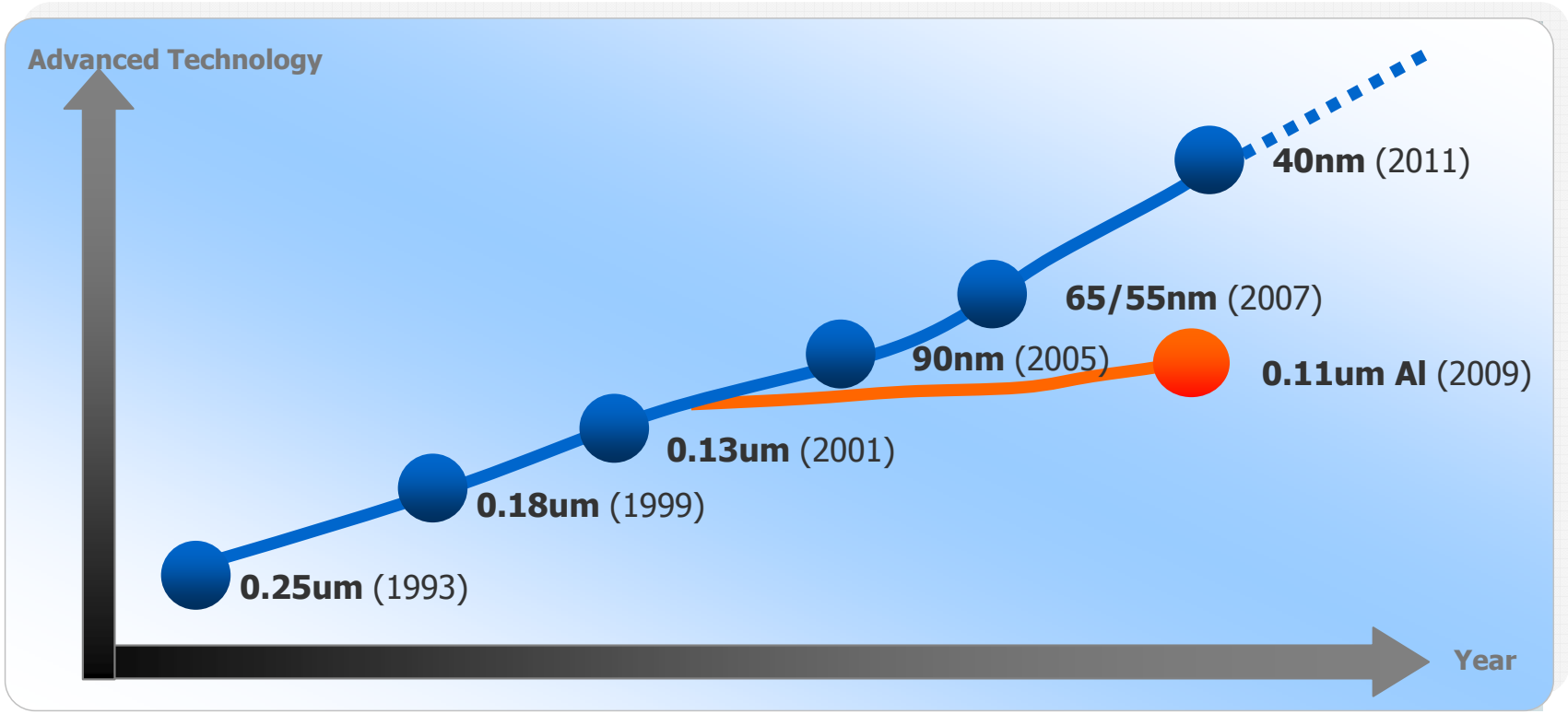
Revenue: US$ millions



Organization



Faraday Technology Roadmap



- Continue to invest in advanced process nodes
- 0.11um Al platform provides cost advantage for non-performance driven applications

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Market Position

RANKING

- **IC design service**
  - WW top 50 fabless house
  - Taiwan top 15 fabless house
- **Silicon IP**
  - WW top 15 IP vendor
  - Taiwan No.1 IP vendor

Note: 2010 IEK data, ranking by revenue

ACHIEVEMNET

- **Most experienced design service company, with**
  - Hundreds of MP projects
  - Millions of chip shipment each year
  - Leader in high-speed IO development
- **One of the most comprehensive /numerous self-developed IPs in the world**

Assisted Customers to Succeed in Market

Area	Application/ Product	Location	Profile
PC peripheral	Flash disk	Taiwan	**No.1 in TWN flash market**
	USB 3.0 host chip	USA	**Pioneer to launch the host solution**
Consumer	Brainwave detector	USA	**Potential chip vendor with customers of ww famous toy/education vendors**
	MFP	Japan	**WW No.1 CE company**
	DSC	Taiwan	**No.1 DSC system maker in TWN**
Display	TV	Taiwan	**No.1 brand in TV market in China**
	Monitor	Taiwan	**No.1 panel maker in TWN**
Communication (Networking)	3G base station	China	**1st tier networking system maker in China**
	Femtocell	Korea	**WW top 5 IDM company**
	Networking security	USA	**WW top 3 vendor in networking security sector**
Audio	MP3	China	**Top 3 MP3 system maker in China**
Video	IP cam, DVR	Taiwan	**No.1 in TWN surveillance market**

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Core Competence to Our Customers' Success

Allow customers to focus on your core competence

IP

- In-house IPs to fulfill 90%+ demand
- Lower the integration risk
- Shorten the lead time
- Enjoy the pricing benefit

TECHNOLOGY

- Platform
  - SoComplier
  - SoCreative!
- Design flow: DFT, DFM, low-power methodology
- Manufacturability: Yield, failure analysis, testing, packaging

SERVICE

- Flexible ASIC business model
- Single window/easy flow to implement till chip delivery
- Foundry partnership
- Co-promotion
- Sales channel & business co-expansion

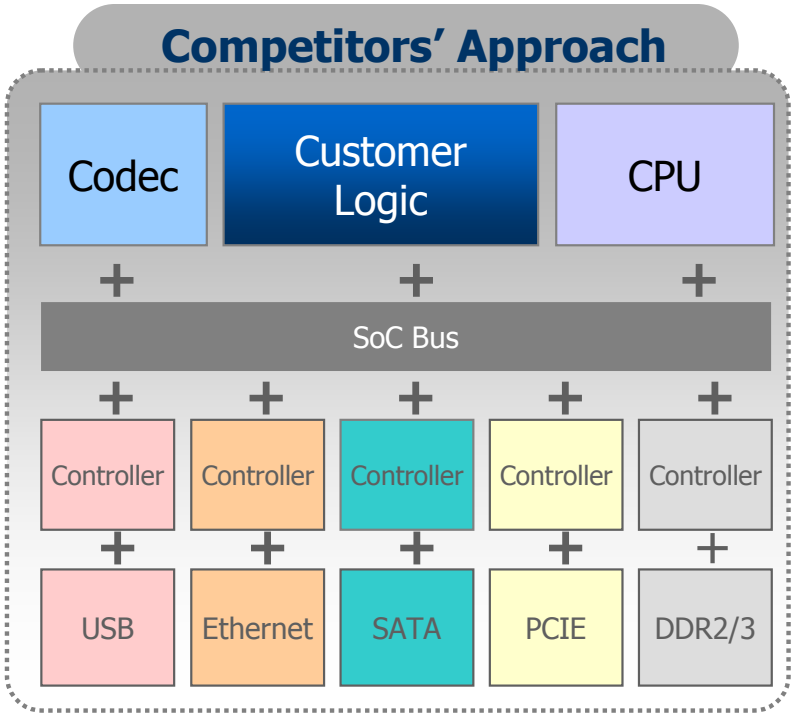
Comprehensive IP Offering

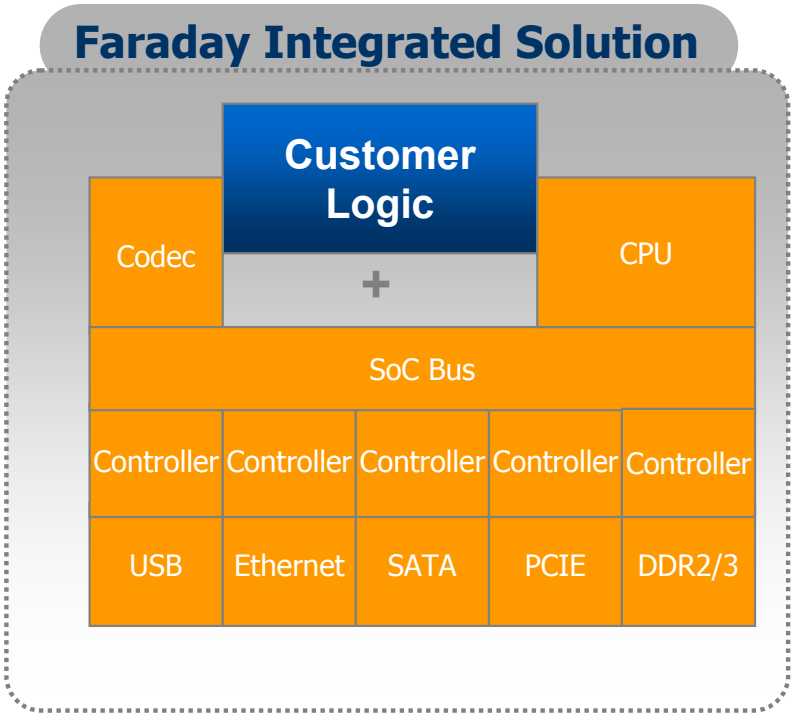
FARADAY

Self-developed IPs

IP

- For advanced SoCs, there has been increasing industry awareness in importance of IP integration
- Faraday has been committed to developing IPs, satisfying more than 90% of customers' requirement on each chip
  - Lower the risk
  - Accelerate the time to market
  - Better cost structure





Comprehensive IP Pool

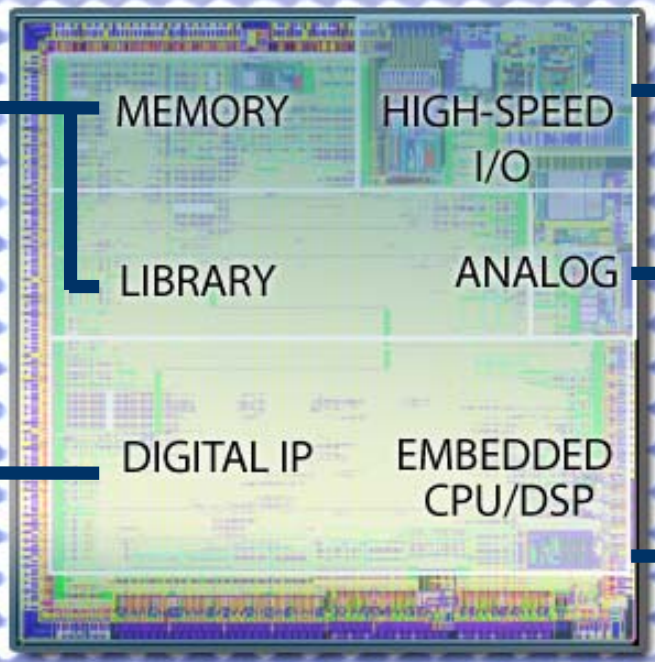
FARADAY IP

MEMORY

- Library / Memory
  - UMC 0.5um - 65nm process standard cell libraries
  - miniLib™: Ultra high density & low power libraries
  - Embedded SRAM, ROM, e-Flash, 1T-SRAM, e-DRAM

DIGITAL

- Peripheral IPs/Controllers/MPEG-4, H.264



HIGH-SPEED I/O

- USB 2.0/3.0, USB-OTG, PCI Express, SATA, Ethernet
- RSDS, LVDS

ANALOG

PLL, SSCG PLL, DLL, OSC, REG, POR, VDT, ADC, DAC, Sigma-Delta ADC/DAC DDD

EMBEDDED CPU/DSP

- DSP: 16/24-bit DSP
- CPU: ARM7/ARM9, Faraday's FA510/FA526/FA626/ FA726TE

Faraday Specialized IP - USB 3.0

IP

- **Positioning**
  - 1st shown in market with industry steering capability
  - The "Reference Host/Device" at USB-IF USB 3.0 Platform Integration Lab
  - USB 3.0 Ecosystem Enabler
- **Success**

"This is a key milestone for SuperSpeed USB and shows progress being made on important components of the USB ecosystem in a short time frame"

Jeff Ravencraft President and Chairman,
USB-IF SuperSpeed USB Developer Conference ,Tokyo, May 22, 2009

Faraday Specialized IP – FA CPU

IP

- **Advantages**
  - One of the few ARM architecture licensees
  - CPU solutions of highest P/E (P/C) in the market
  - Complete CPU solutions from low- to high-end
- **Success**

Application	Core	Customer profile
Femtocell	FA626TE	WW top 5 IDM company
Video Surveillance/DVR/NVR	FA626TE/ FA606TE	Tier one vendor in Korea
Networking	FA626TE	Tier one company in USA
KVM	FA626TE	Tier one PC/NB vendor in USA
DSC	FA510	Tier one TWN based DSC ODM/OEM
Network Security	FA626TE	Tier one supplier of encryption technology in US
MP3/PMP/SSD	FA606TE	TWN local brand

Besides In-house IPs,

- **Provide one-stop shopping service with 3rd party IPs**
- **Close relationship with strategic IP partners**
  - Assist customers to penetrate into niche market with unique IPs via strategic IP partners:
    - Ex. Security algorithm, decryption methodology, Display port
  - Assist IP partners to get access to emerging markets

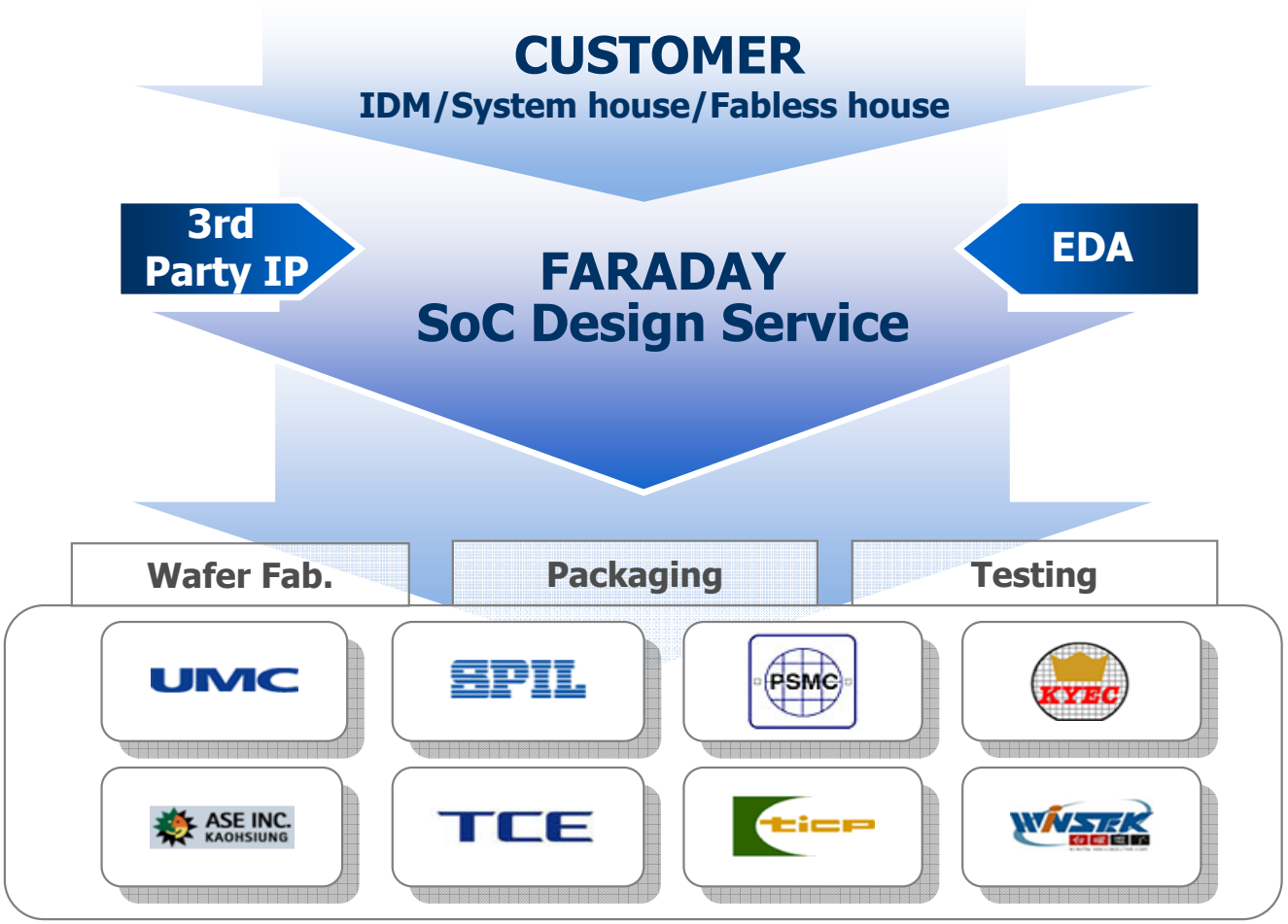
More partners are listed on FARADAY web site

High Quality Services

FARADAY

One-stop Shopping for Customers

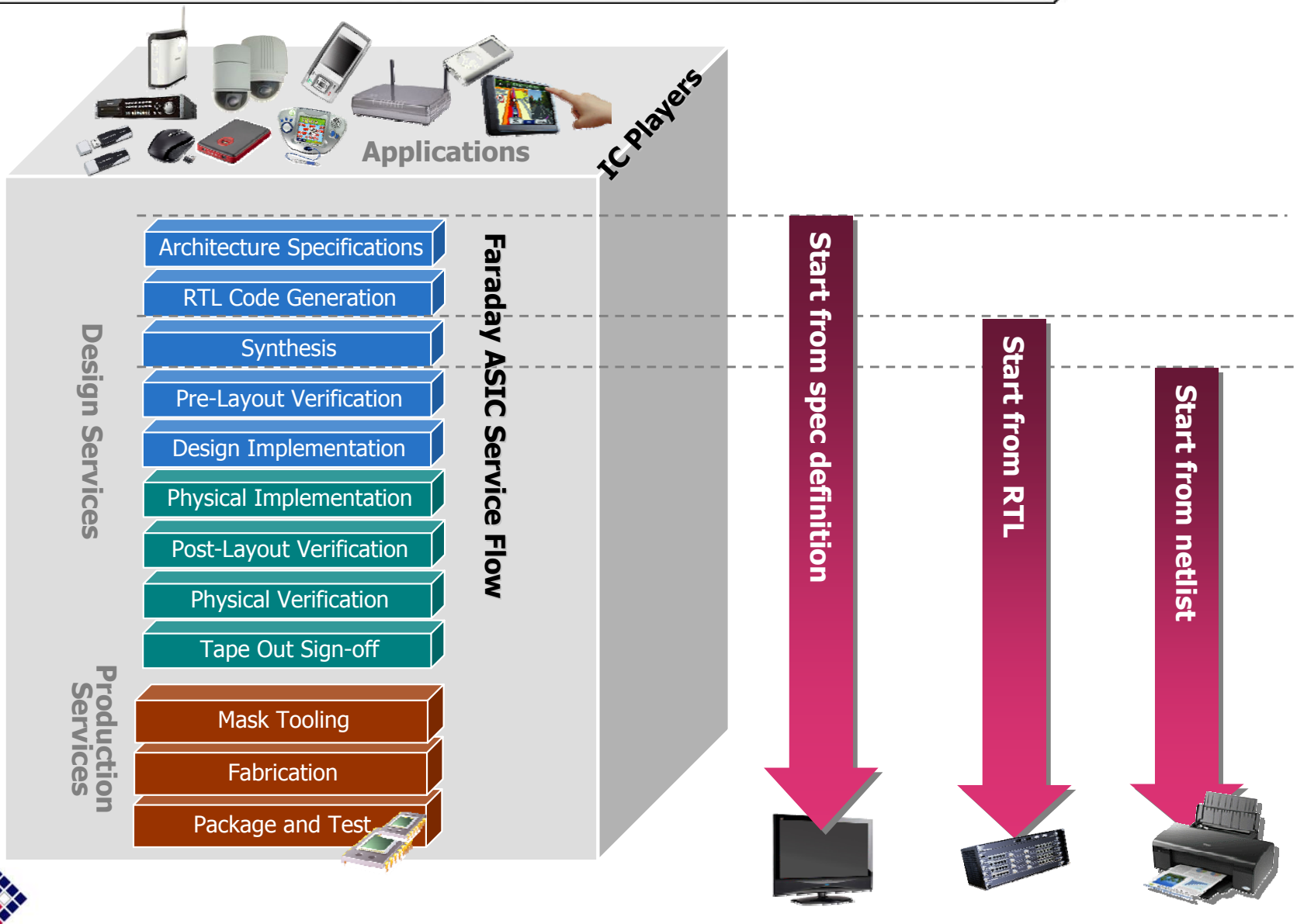
Service



- Close co-work with foundry to ensure process familiarity
- Multiple subcontractors for quality, efficiency and risk control

Flexible Business Model

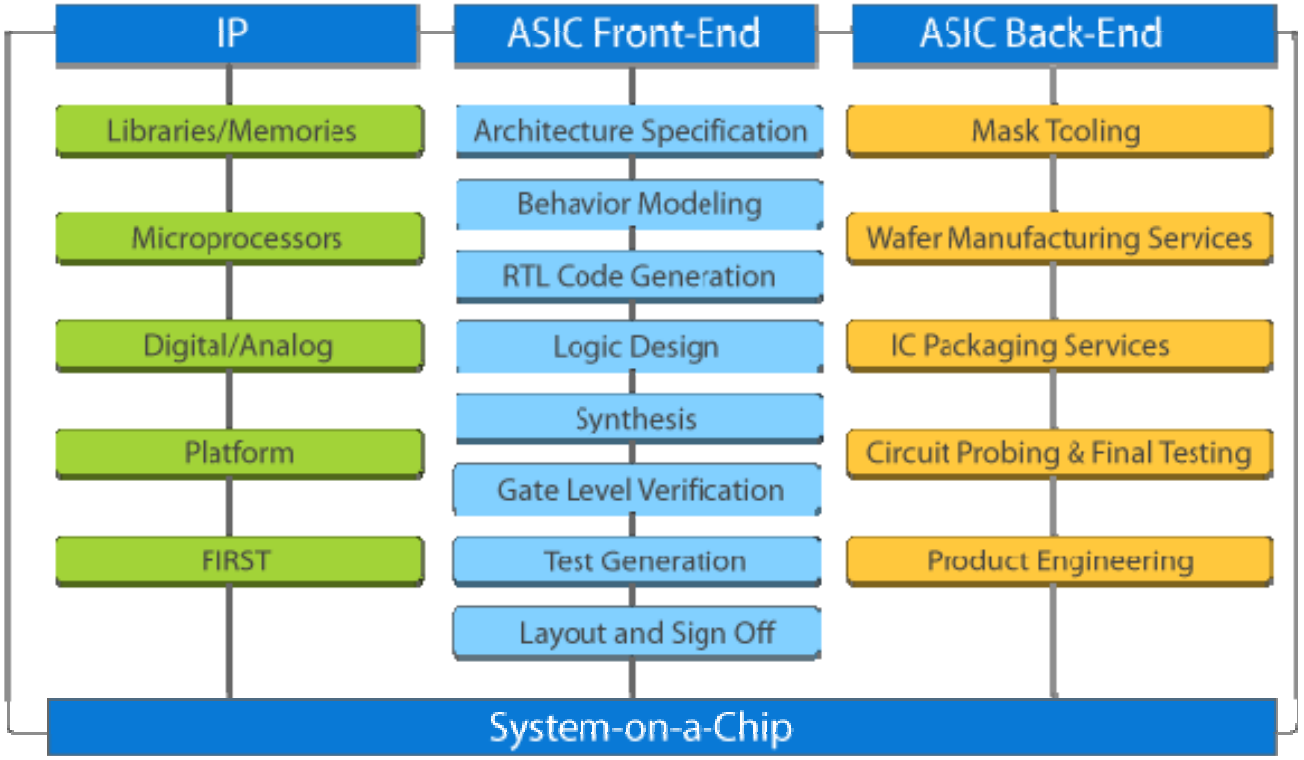
Service



From Design to MP, Faraday Makes It A Simple Flow!

Service

FARADAY SOC DESIGN SERVICE



- Infrastructure : People, equipment and IT
- Expertise : Test development & convergence/Yield improvement/ Failure analysis

Excel Your Idea to Silicon

Front- & Back-end Technology to Ensure Your Competitiveness

FARADAY

Front-end & Back-end Technology

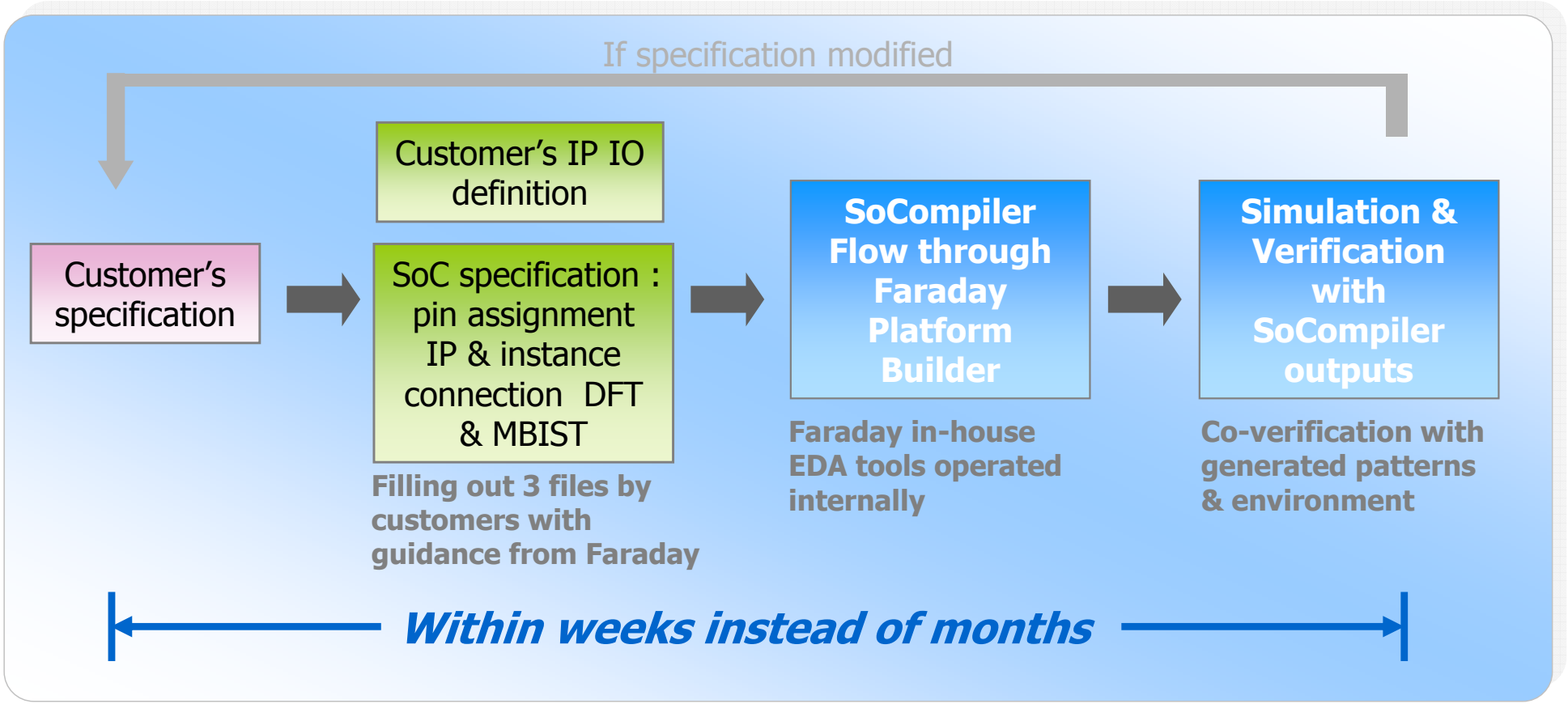
Tech

Stage	Benefit	Core
SoC platform	❖ To reduce customers' integration efforts for fast time-to-market ❖ To provide reliable modules connection, preventing manual incorrectness	SoCompiler, SoCreative!
Design methodology	To assure customers' product be more reliable and more power-saving	❖ Power integrity solutions ❖ Chip, package, and PCB co-design solutions ❖ SiP BIST solutions ❖ Lower-power solutions
Testing	❖ Shorten ES verification and debug turnaround time ❖ Test platforms to provide cost-down path	❖ Testing capability covers from mixed signal IP, HSIO to CPU ❖ Provide cost down path when volume ramp up
Manufacturing	One-stop and seamless (in-house) flow to improve the yield rate	❖ Process control & analysis ❖ Solid relationship with the foundry and vendors throughout the flow

SoCompiler! SoC Platform

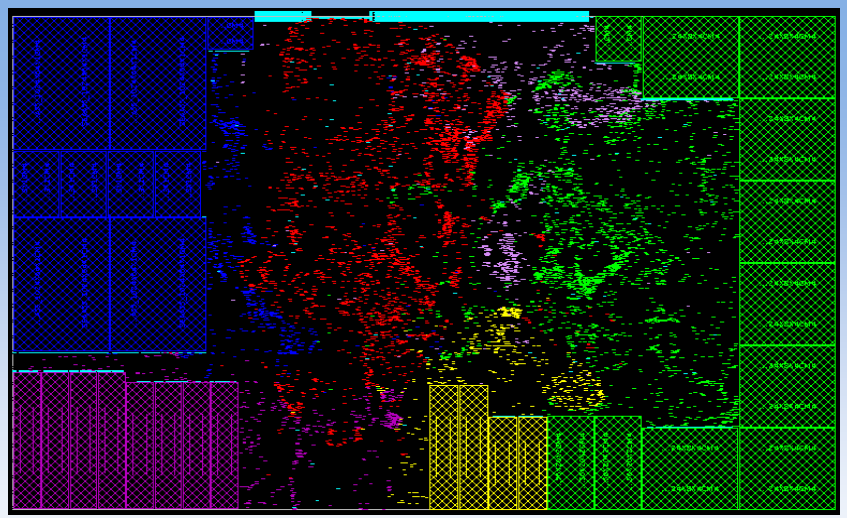
Tech

- Shorten SoC design cycle time
- Provide a comprehensive verification environment to reduce risk



Design Methodology

- Robust design methodology to assure reliable and power-saving design and shorten lead time
- Success case:



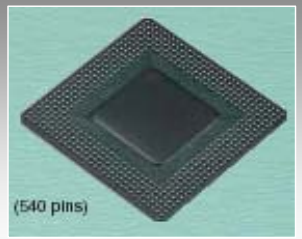
- Application: Femtocell
  - Process: 65 nm (1P8M2G)
  - Gate count: 22M
  - Frequency: 800 MHz (Max.)
- Specialty: At-speed MBIST
- Lead time: SoC platform integration- 8 weeks
- First-cut work

Manufacturing

Tech

Wafer

Package



Testing

Production

- Familiar with UMC process
- Long-term partnership to get better support in wafer allocation, and engineering support

- Work with 1st tier package houses for fast time-to -market
- Qualify 2nd tier package houses for cost down and capacity allocation
- Substrate design covers bonding diagram, substrate layout and ball assignment
- Take BOM, thermal effect, SI, etc into account when doing package design

- In-house testers, to shorten ES verification and debug turnaround time
- Different test platform provide cost down path
- Generate test plan for 3rd party IP as well

Faraday News

[中央社記者張建中新竹2011年3月23日]

- IC 設計服務公司智原科技 (3035) 董事會今天決議，營運長 臧維新 升任總經理一職；總經理 林孝平 將轉任副董事長。
- 業界人士表示，智原董事長 宣明智 未來應會交棒予 林孝平；林孝平 轉任副董事長一職，應是暫時的安排。

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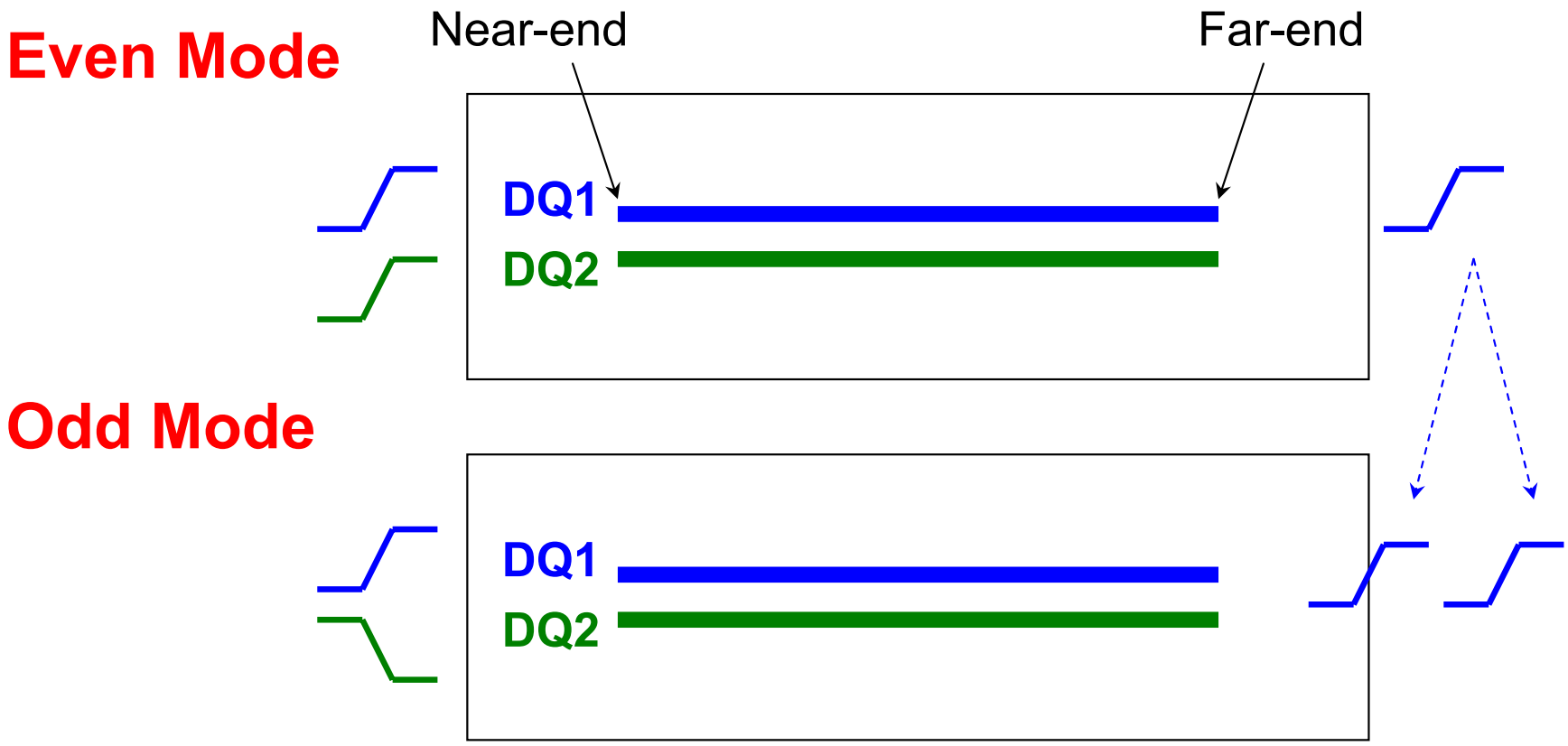
What is “System Signal Integrity” ?



❖ **Which one will reach the far-end earlier ?**
(Even mode or Odd mode)

Maxwell Equations

Beyond "Noise = IR + L di/dt"

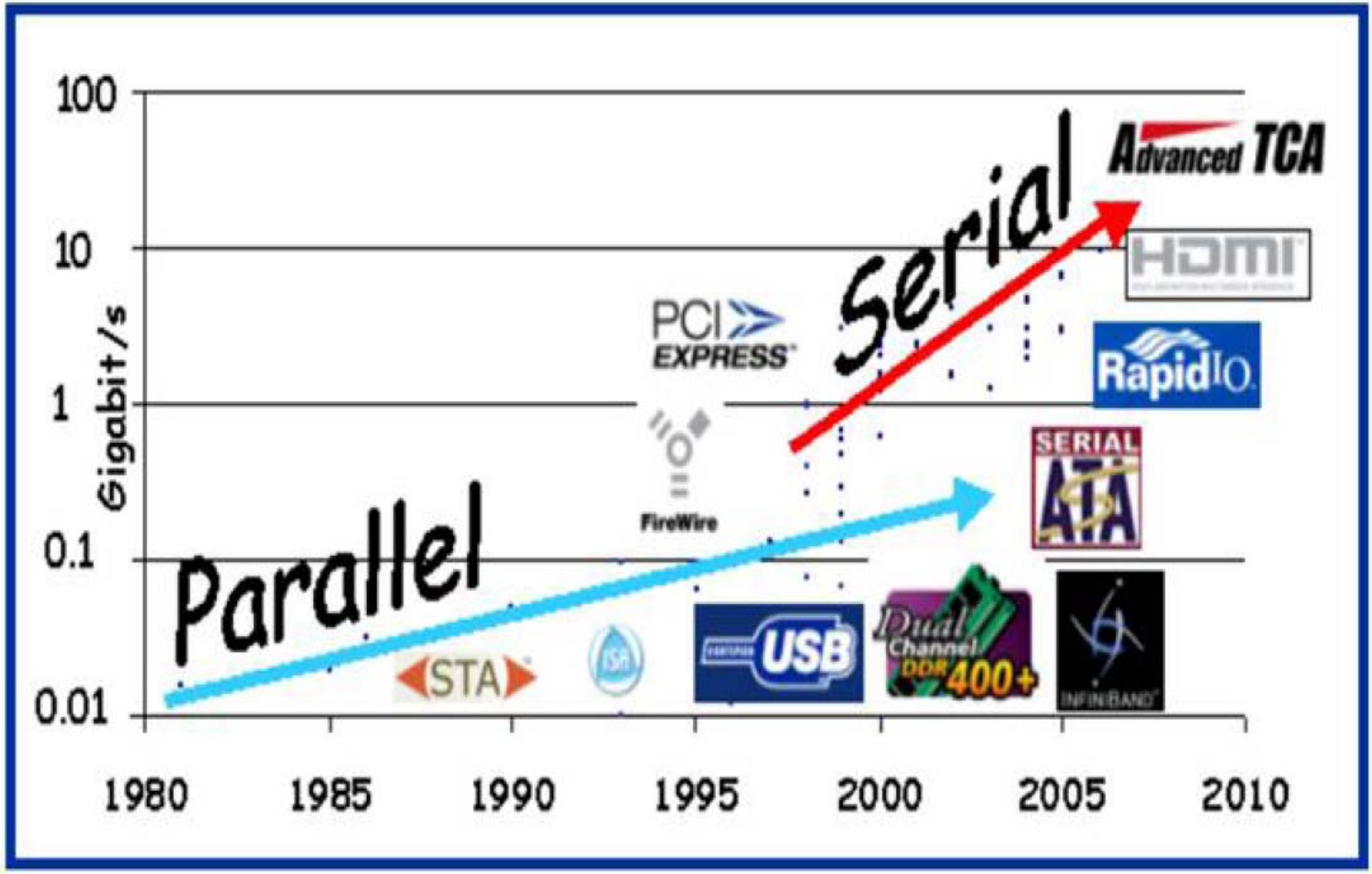
$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}$$

$$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t}$$

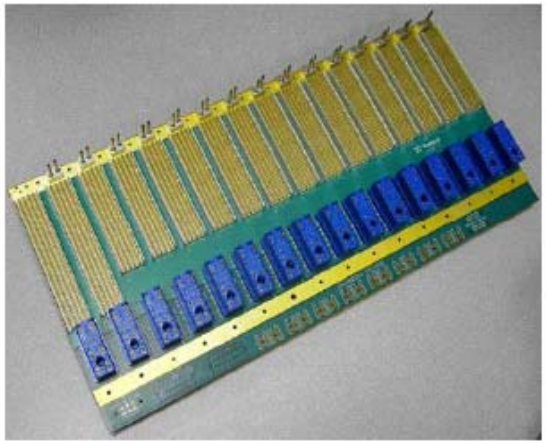
$$\nabla \bullet \vec{D} = \rho$$

$$\nabla \bullet \vec{B} = 0$$

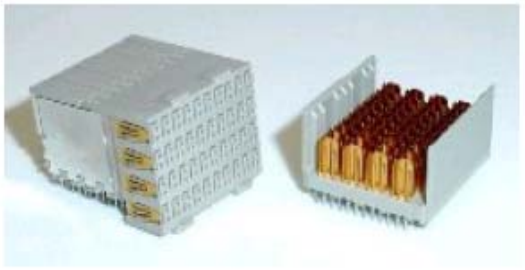
Signal Integrity is Challenging



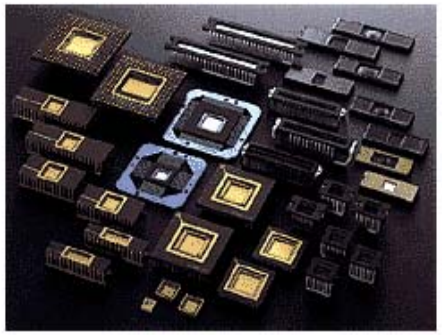
Impedance Problems are Everywhere



Backplanes

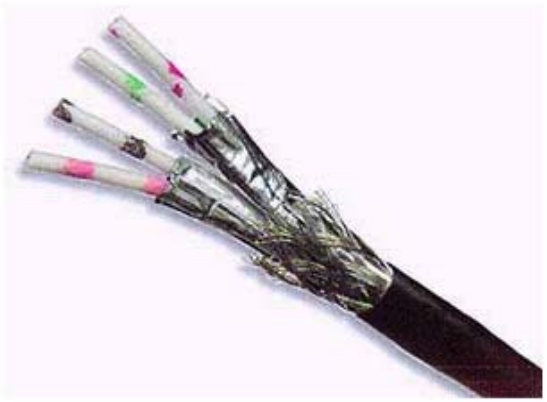


Connectors



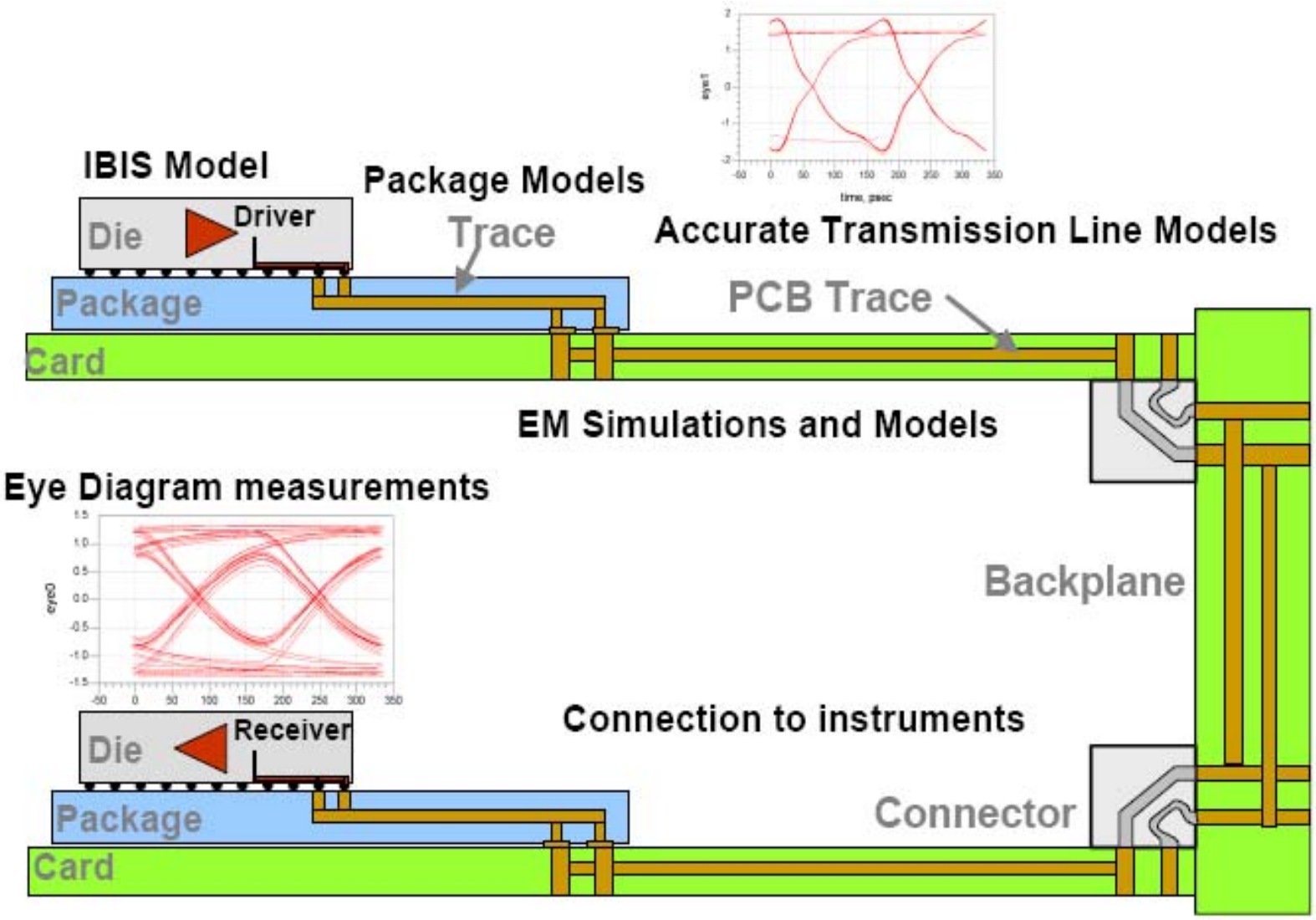
IC Packages

PC Boards

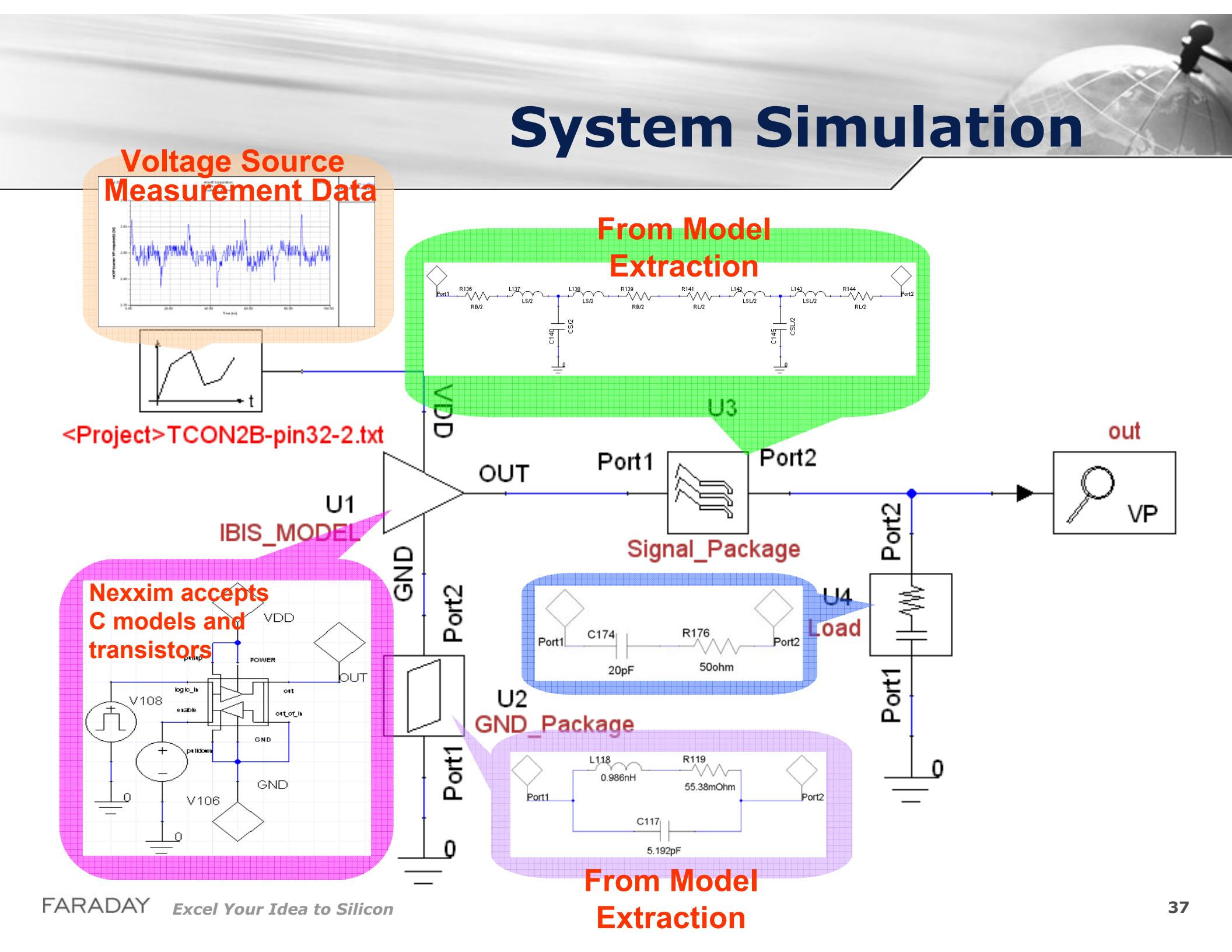


Cables

IC/PKG/PCB Co-Design

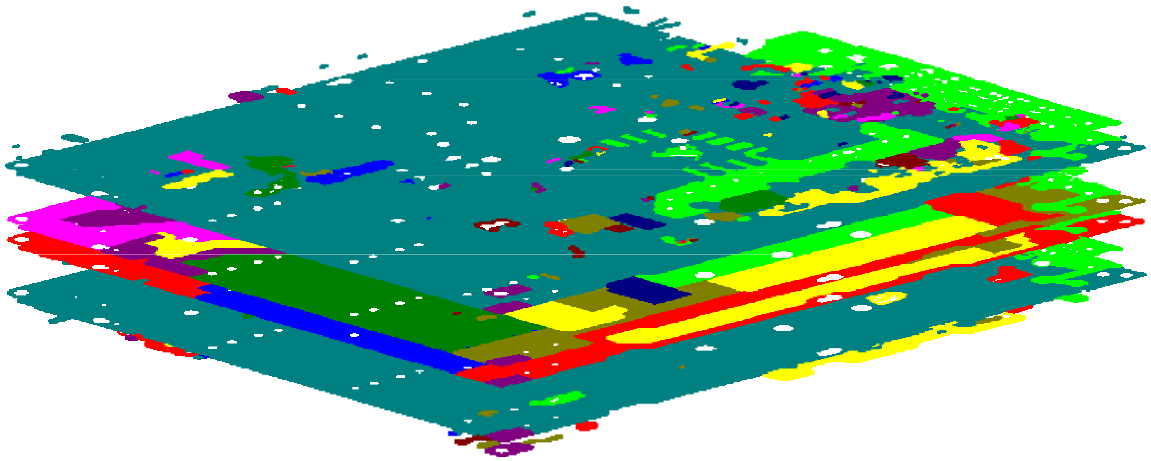


System Simulation

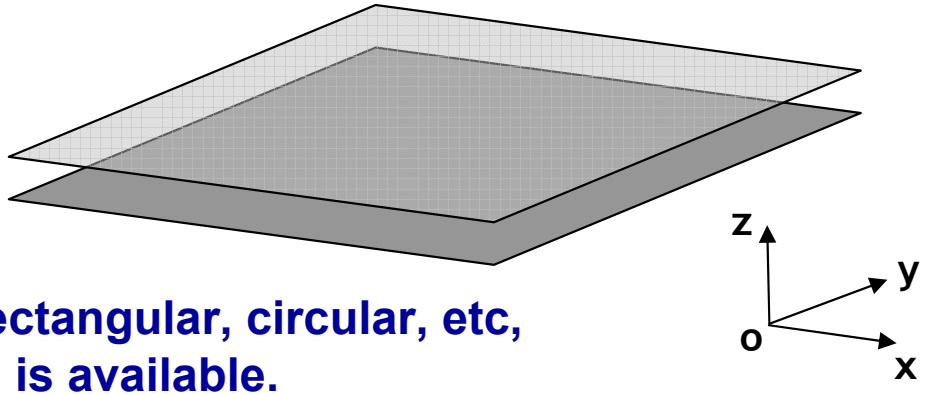


EMI Problem on PCB/Package

PCB plane resonance



A PCB usually contains multiple planes for providing lower impedance between power and ground

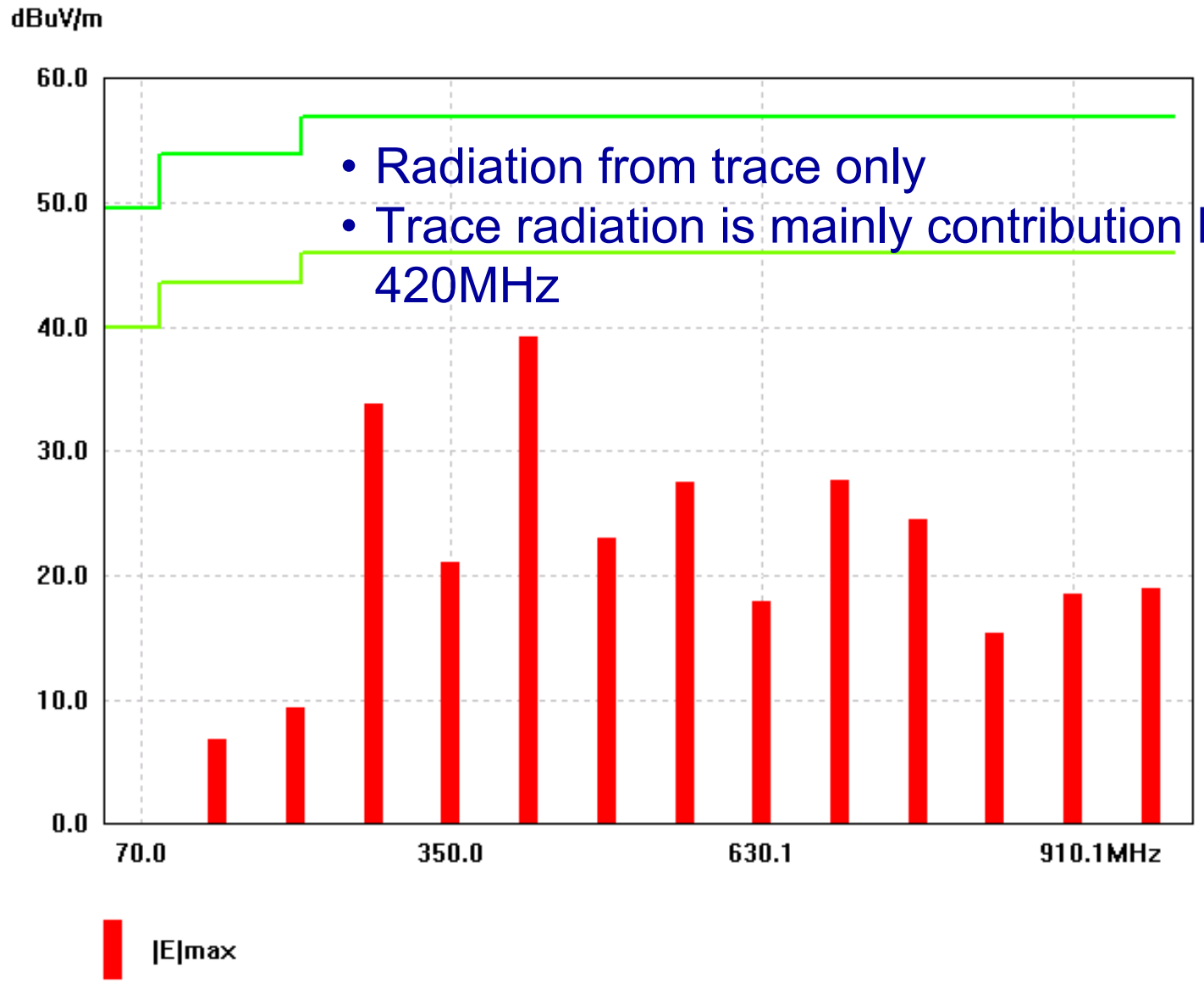


Usually, parallel plate model is used in modeling.

For several regular shapes, such as rectangular, circular, etc, analytical solution of field distribution is available.

However, for arbitrary shapes and various edge loading conditions, numerical solution is practically used in engineering.

EMI Simulation



- Radiation from trace only
- Trace radiation is mainly contribution below 420MHz

History

- **In 2006/Q1, we started to evaluate the system SI tools and EM tools and to built up the related capability**
- **In 2006/Q4, we purchased the tools**
  - Cadence: Allegro630, Allegro Package Design
  - Ansoft: Nexxim Designer, HFSS
  - Sigrity: PowerSI, Broadband SPICE
- **In 2007/Q1, we announced that we can do the system SI analysis by ourselves**
- **In 2007/Q4, we formed the high speed co-design task force to face the new challenges**
- **In 2010/Q1, we purchased Sigrity-XtractIM to extract high pin count BGA models**

High Speed Co-Design Task Force (SI, PCB, PKG, IP)

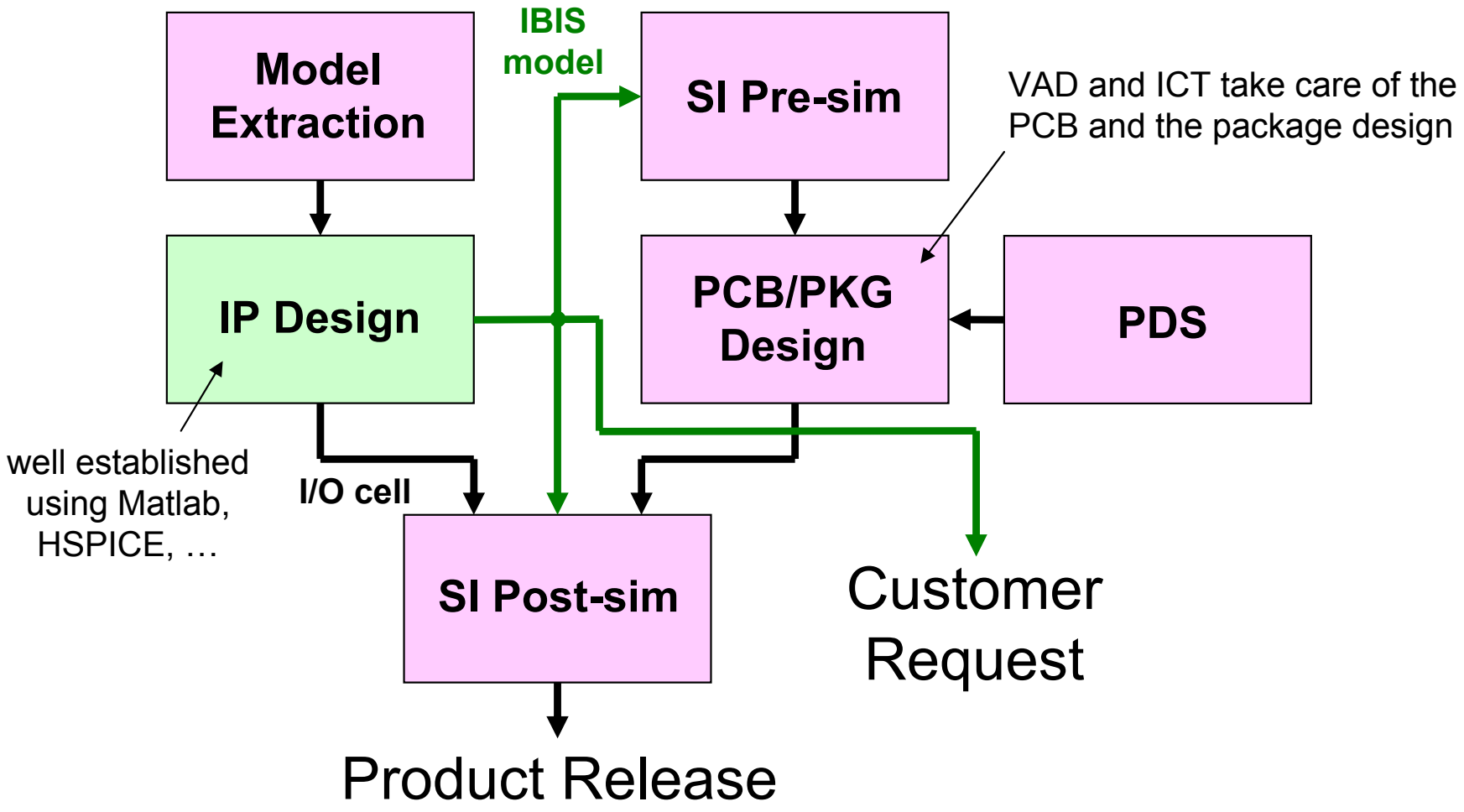
- ASIC Failure Rate Due to substrate design: **2007 -> 4/37, 2008 -> 0/34**
- Designed in 2007
  - FZC0AA033A
  - FFA0AA026001AE
  - FFC0AA028AB
  - FSA0AC191AB

Value Added Services

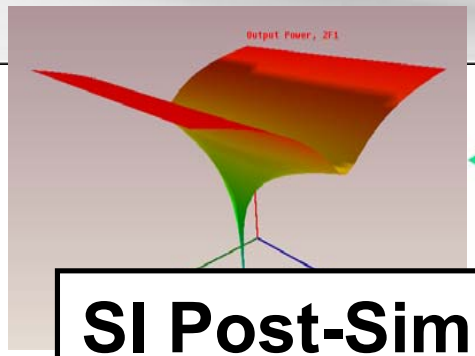
We can

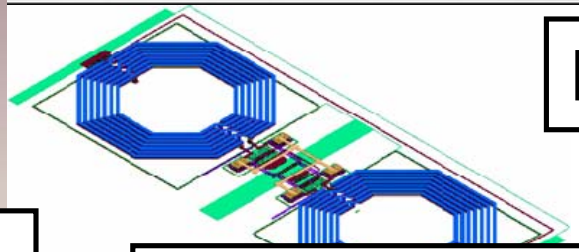
- Help our customers to optimize the de-coupling capacitors and to ensure the power/ground quality of the PCB → PDS (power delivery system) analysis
- Give customers some layout (trace, via ..) guidelines on PCB → SI pre-sim
- Deliver the models of package (PKG) and PCB for design validation → 2D/3D models extraction
- Help our customers to simulate the whole system after IC, PKC and PCB are integrated and also provide the debugging services → SI post-sim
- Design the customized high speed package (including substrate & SiP) → package design capability

Total Solutions to System SI

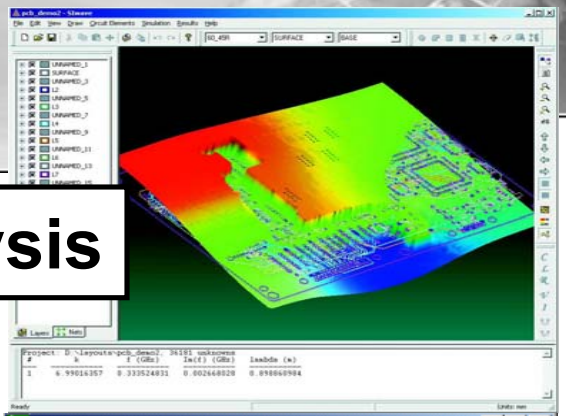


Five System SI Solutions

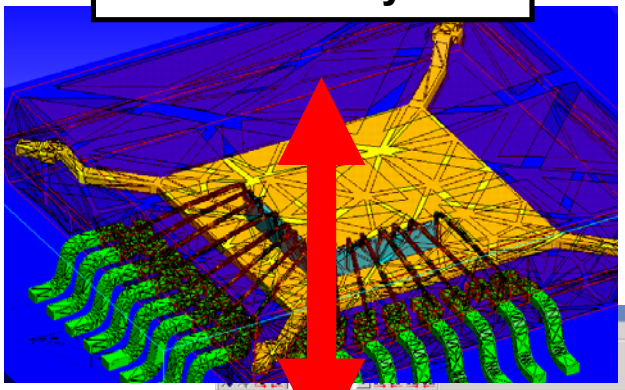




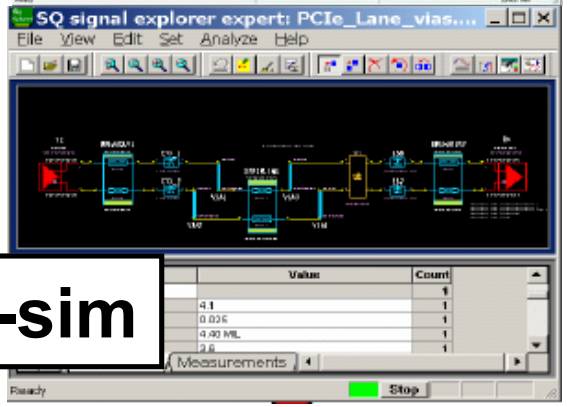
PDS Analysis



SI Post-Sim
1. EMI Analysis

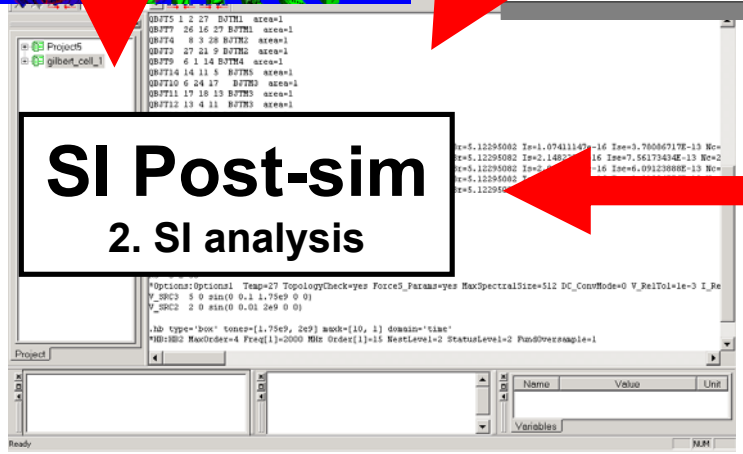


Model Extraction
(R/L/C, S-par.)

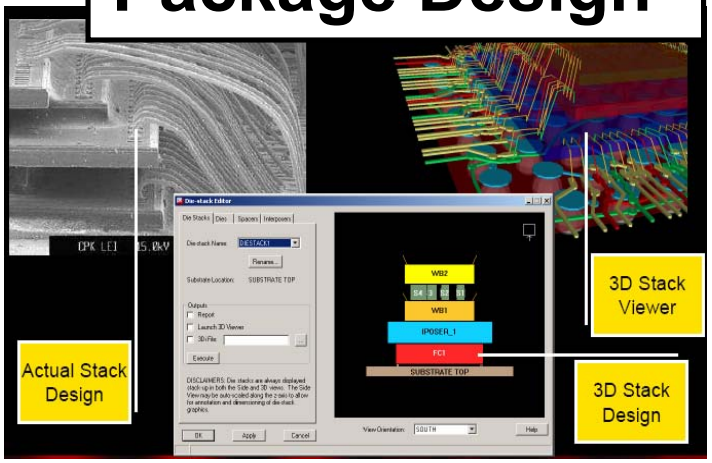


SI Pre-sim

SI Post-sim
2. SI analysis



Package Design

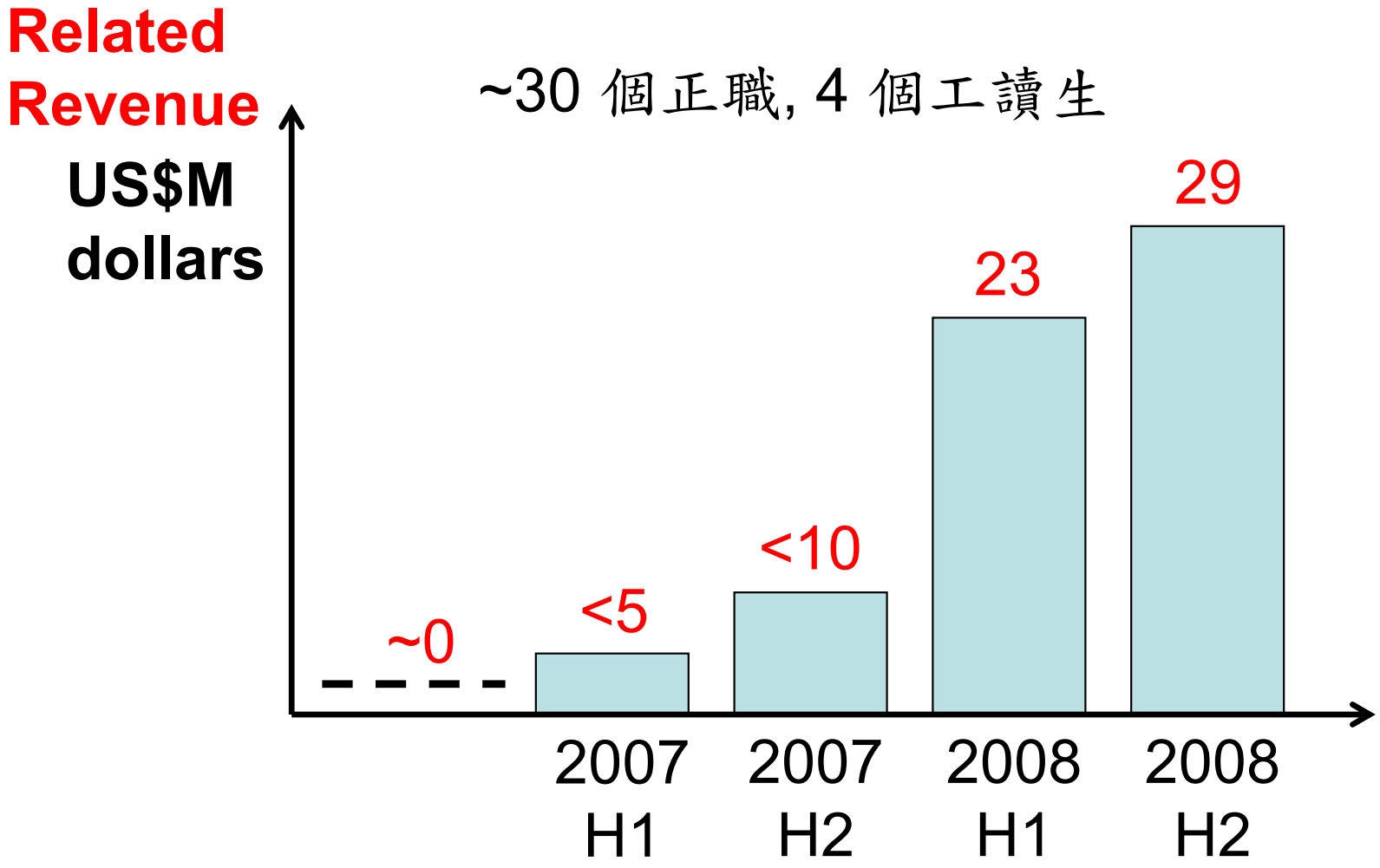


Infra-structure R&D Center (2005~2009, 1/2)

- **New ESL Methodologies**
  - Multimedia Virtual Platform for software porting and debugging
  - Next Generation MPCore ESL Design for hardware exploration
- **Design for Testability**
  - Programmable Memory Built-in Self Test enables BISR System, Memory Compiler, URAM BIST, ASIC Debugging
  - Test Methodologies for Special IPs (Jitter Measurement, CODEC BIST, …)
- **Digitized Analog Designs** (AD-PLL, SSCG, FN-PLL) with very small area (5%~20%) and short time-to-market (1/4~1/2)
- **Next Generation Library** for high speed variation tolerance design
- **Analog Synthesis Automation Platform (ASAP)** speeds up analog design & porting 1.5x~5x
- **High Speed Co-Design Task Force** is carrying us from analysis, simulation, debug to prevention
- **Advanced ESD solutions** are being investigated for low area, low capacitance and low leakage
- **Key Problem Solving** for CRD test chip improvement
  - USB reliability issues - NBTI
  - ESD layout checker
  - CAD issues

Infra-structure R&D Center (2005~2009, 2/2)

~30 個正職, 4 個工讀生



Agenda

- **Introduction**
  - Faraday profile
  - Market position
  - Core competence
- **System Signal Integrity**
- ***Case Studies***
- **Summary**

Case 1

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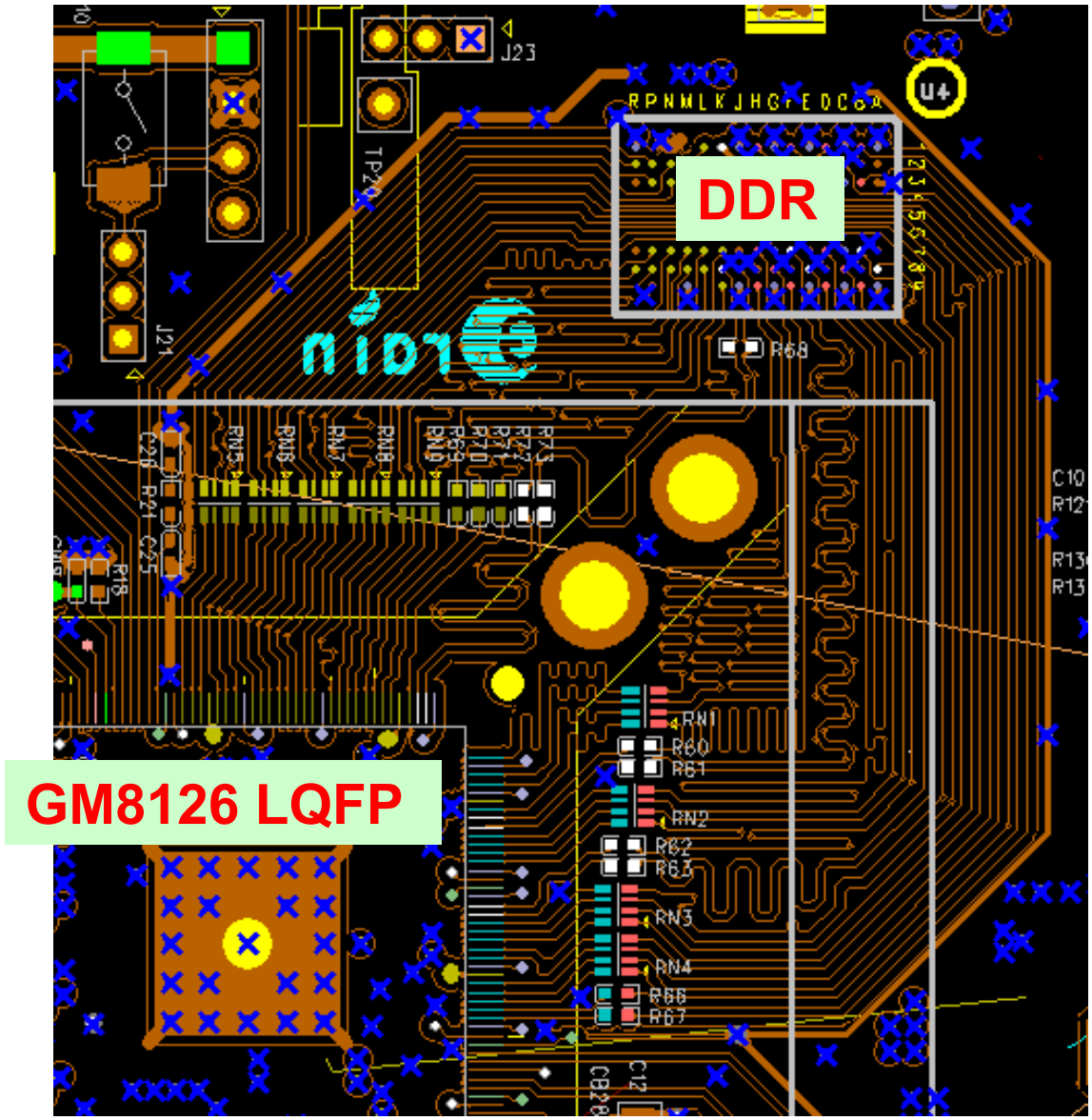
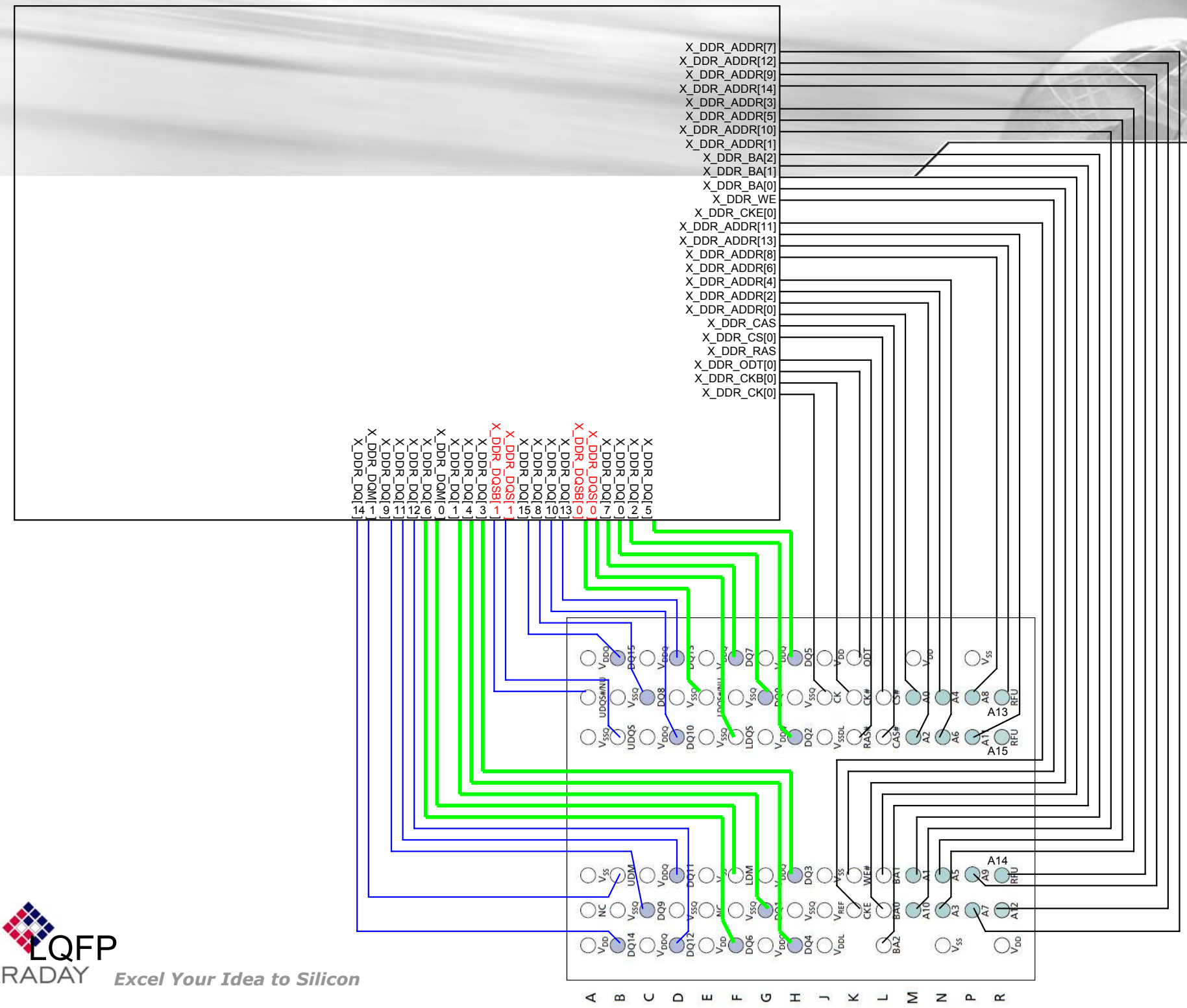
PCB Layout Topology (4 layers -> 2 layers)

GM8126 LQFP

PCB pin sequence
-> Package
-> IP pin sequence





LQFP

FARADAY *Excel Your Idea to Silicon*

Case 2

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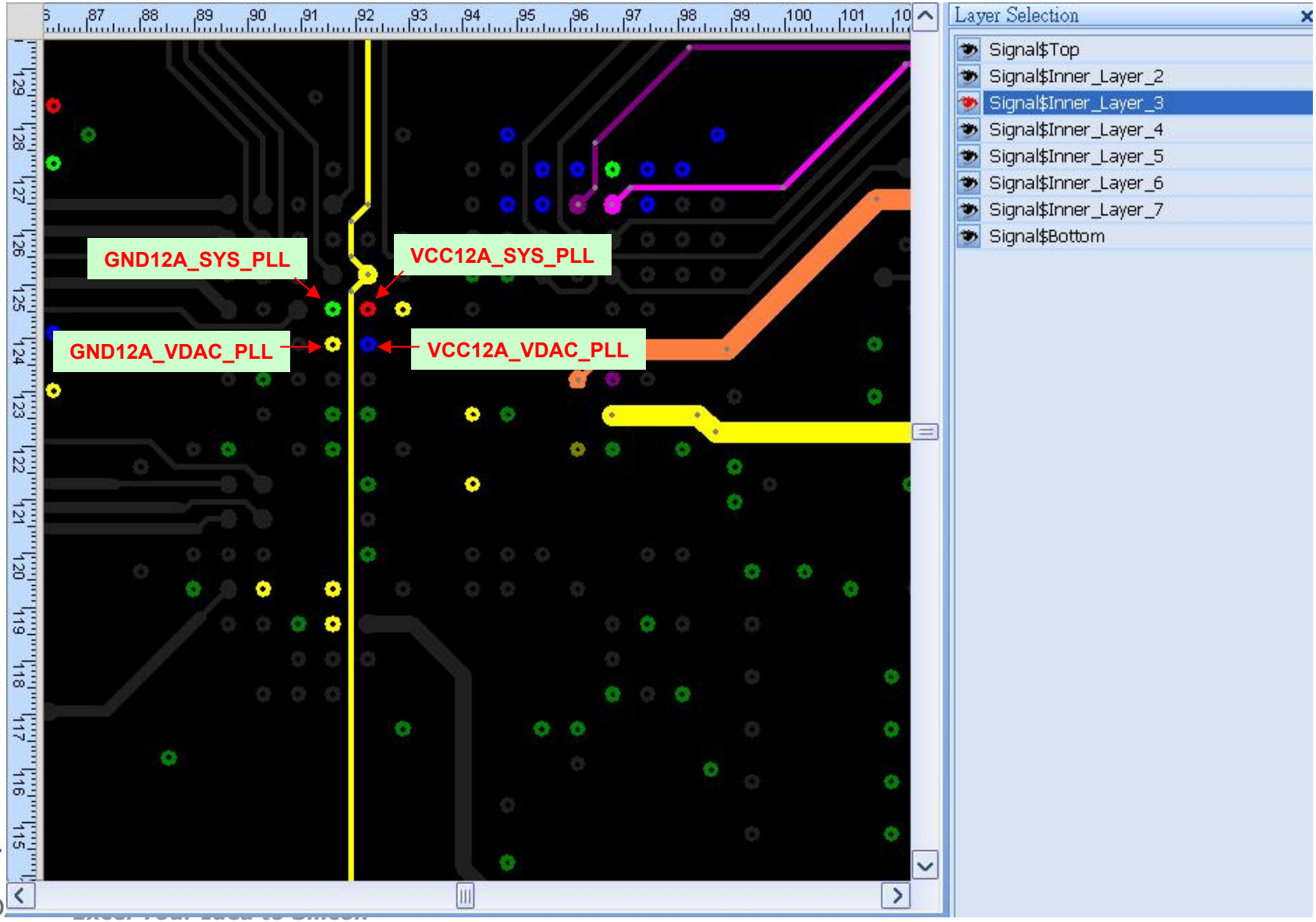
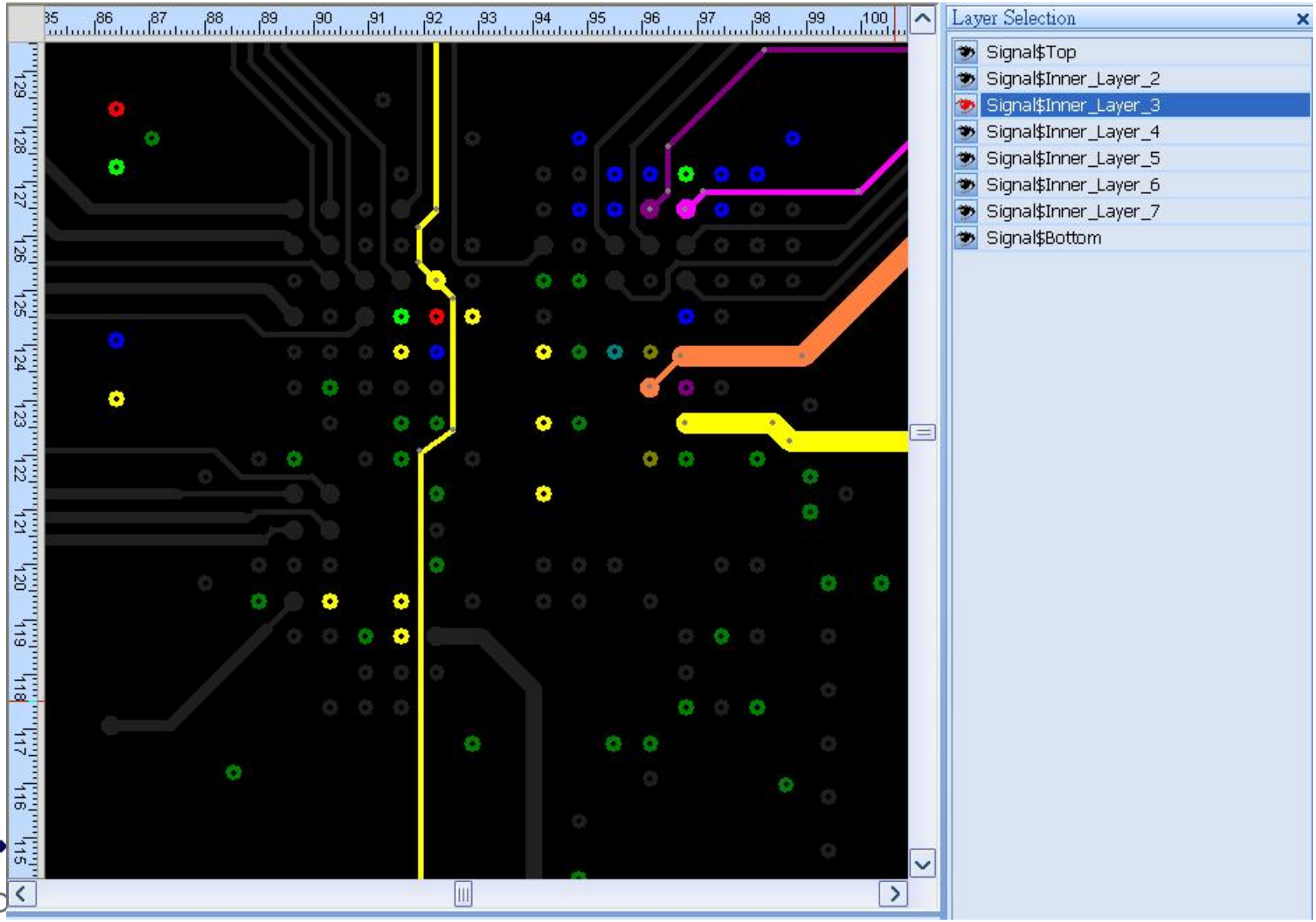
Original PCB Layout

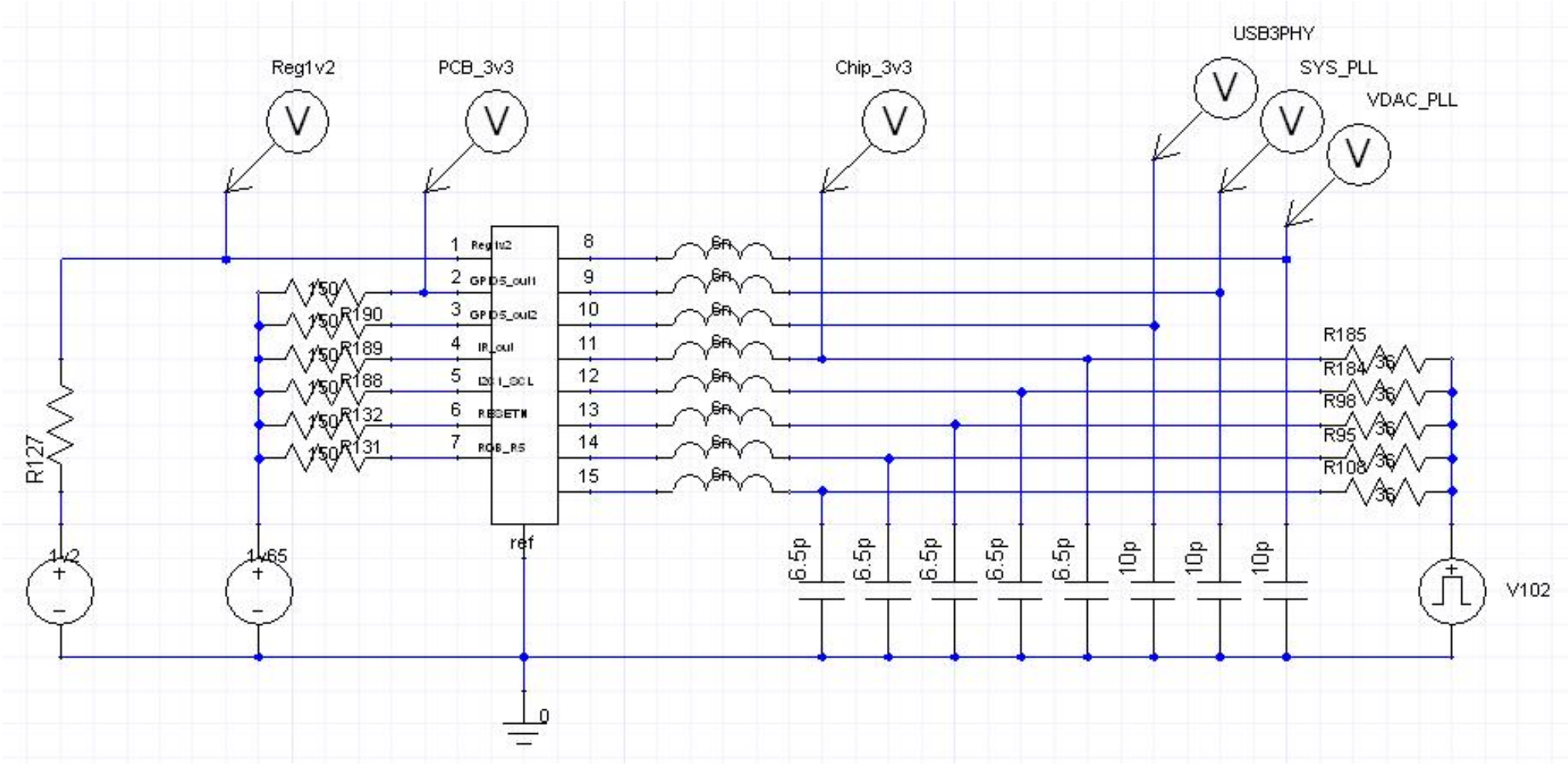


Modified PCB Layout

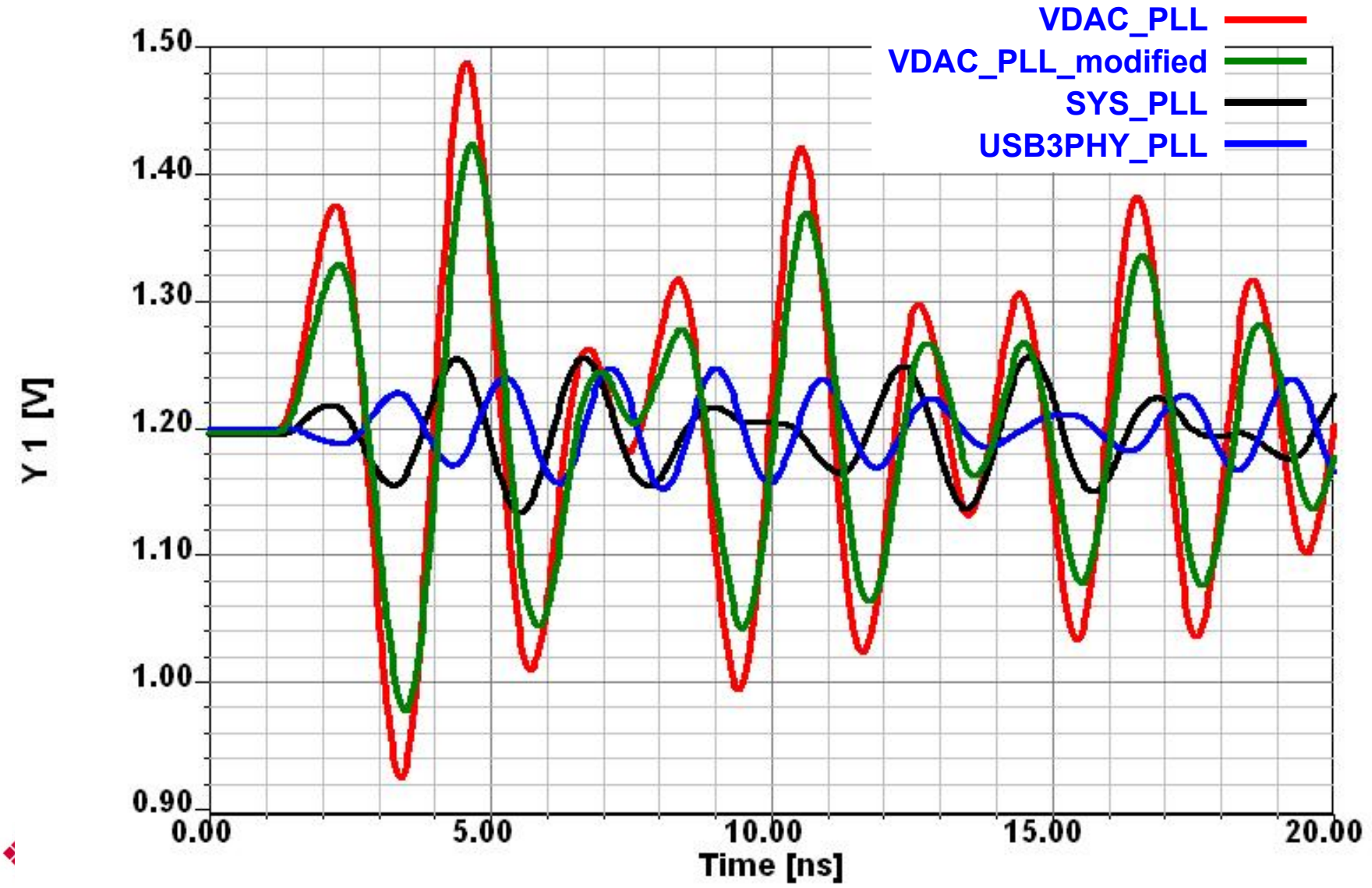


FARAD

Schematic of Coupled I/O



The noise on VDAC_PLL can be reduced around 20%



Case 3

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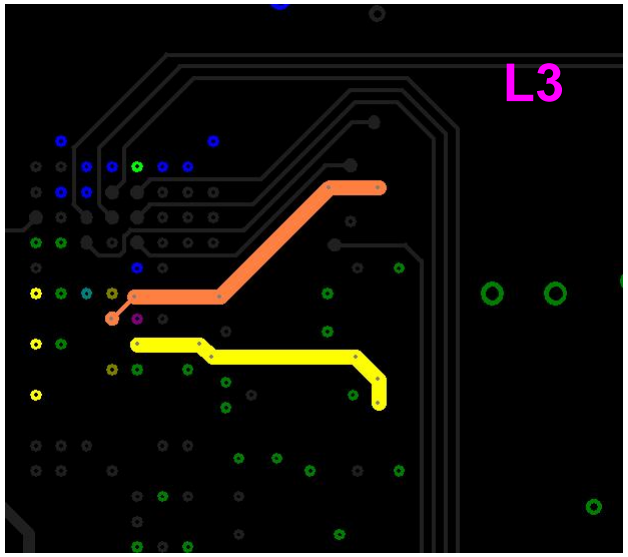
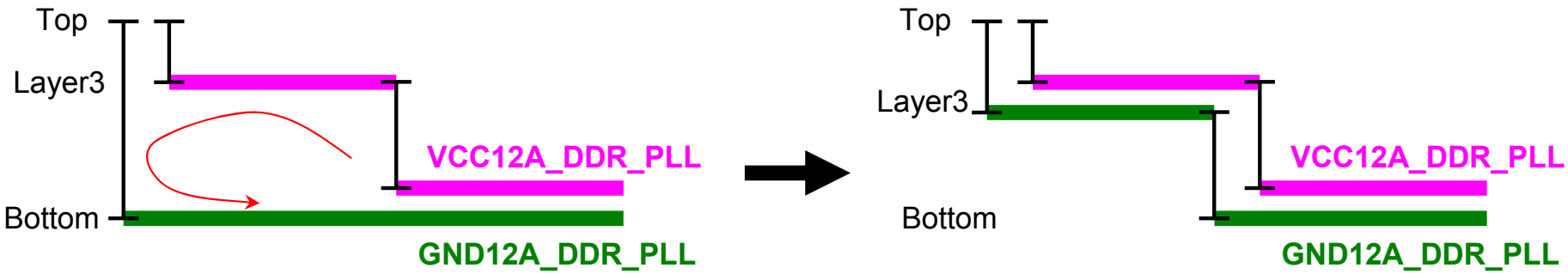
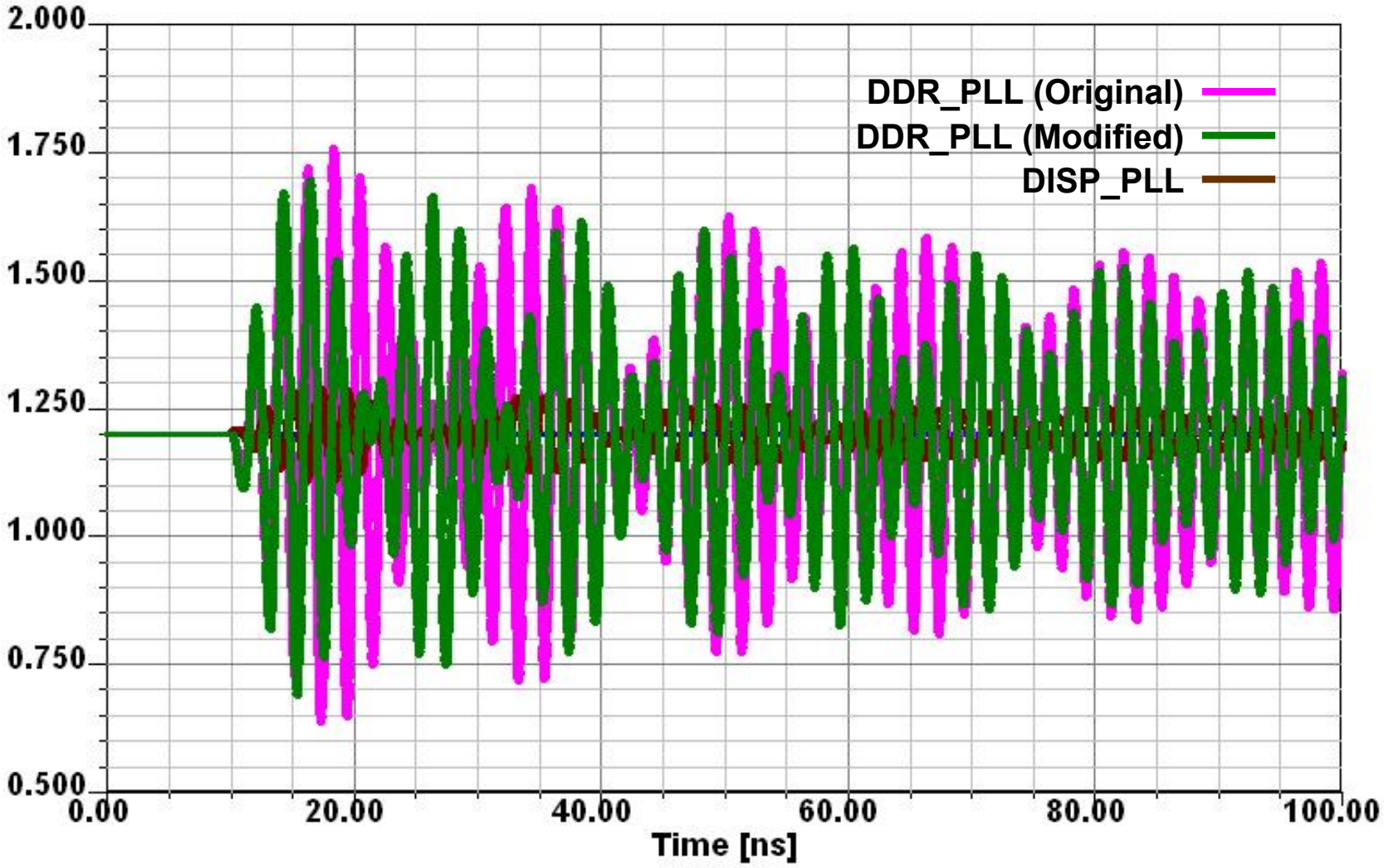
The Loop Concept



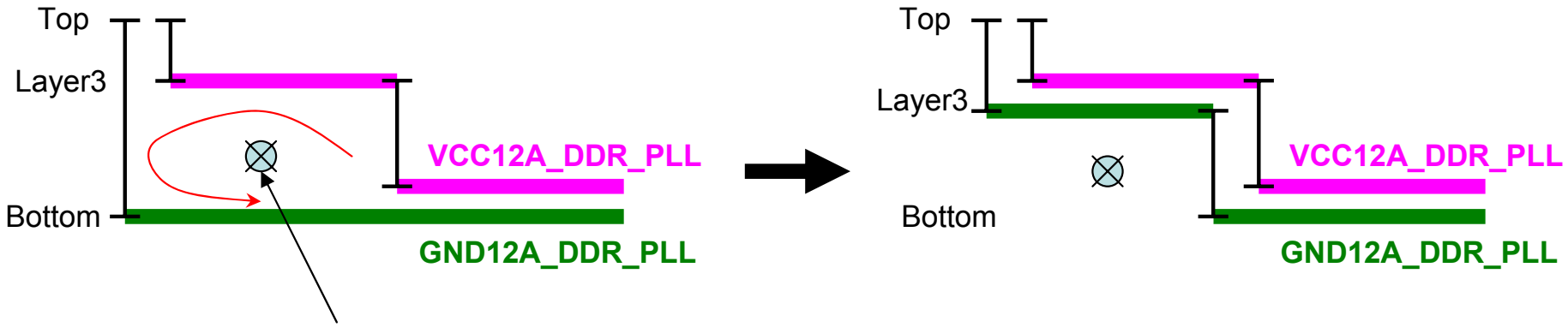


Simulation Result Coupled by the Neighbor Signals
(SPI_MOSI, SPI_MISO, SPI_DATA2, SPI_CLK)

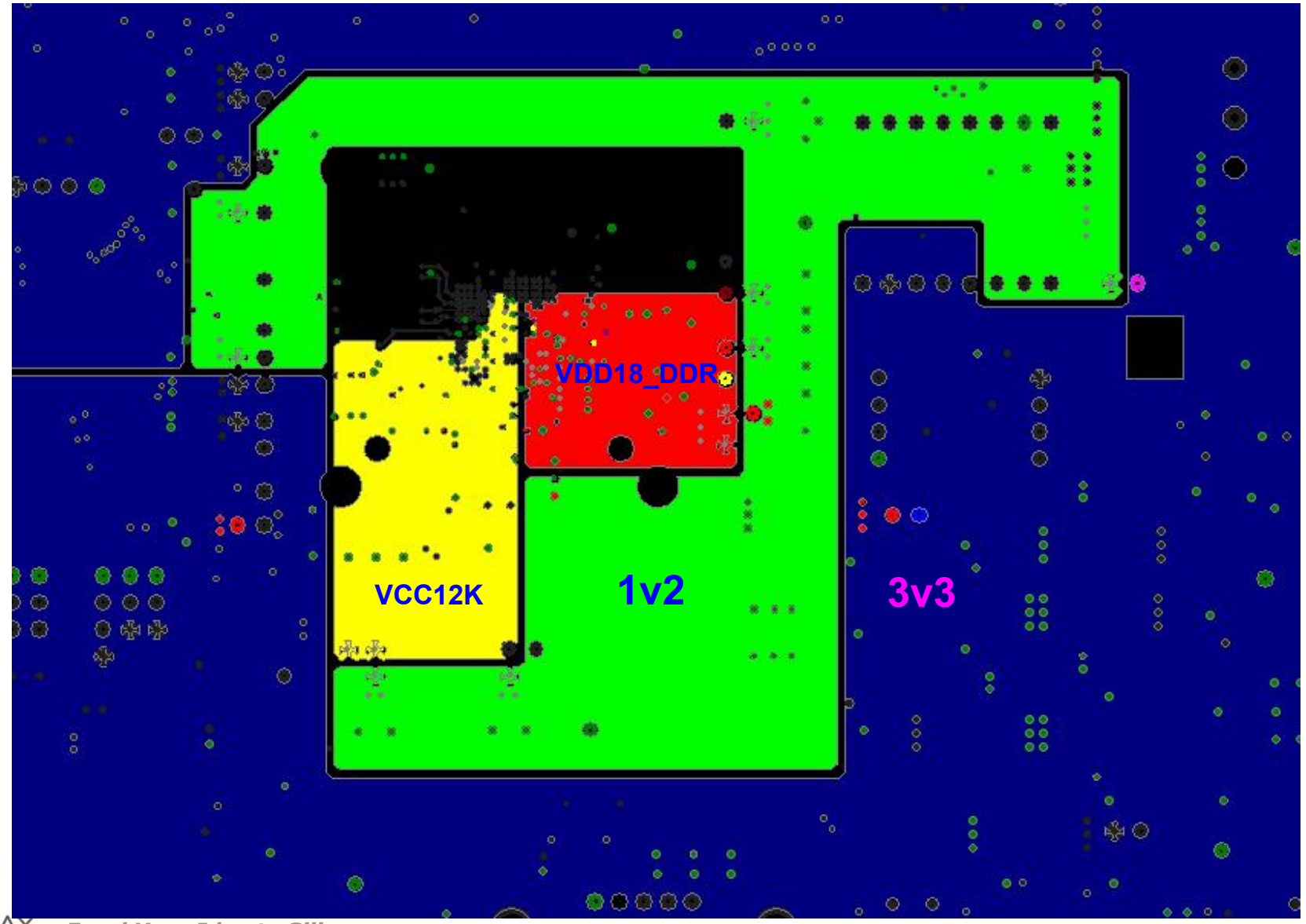


The Effect in This Case

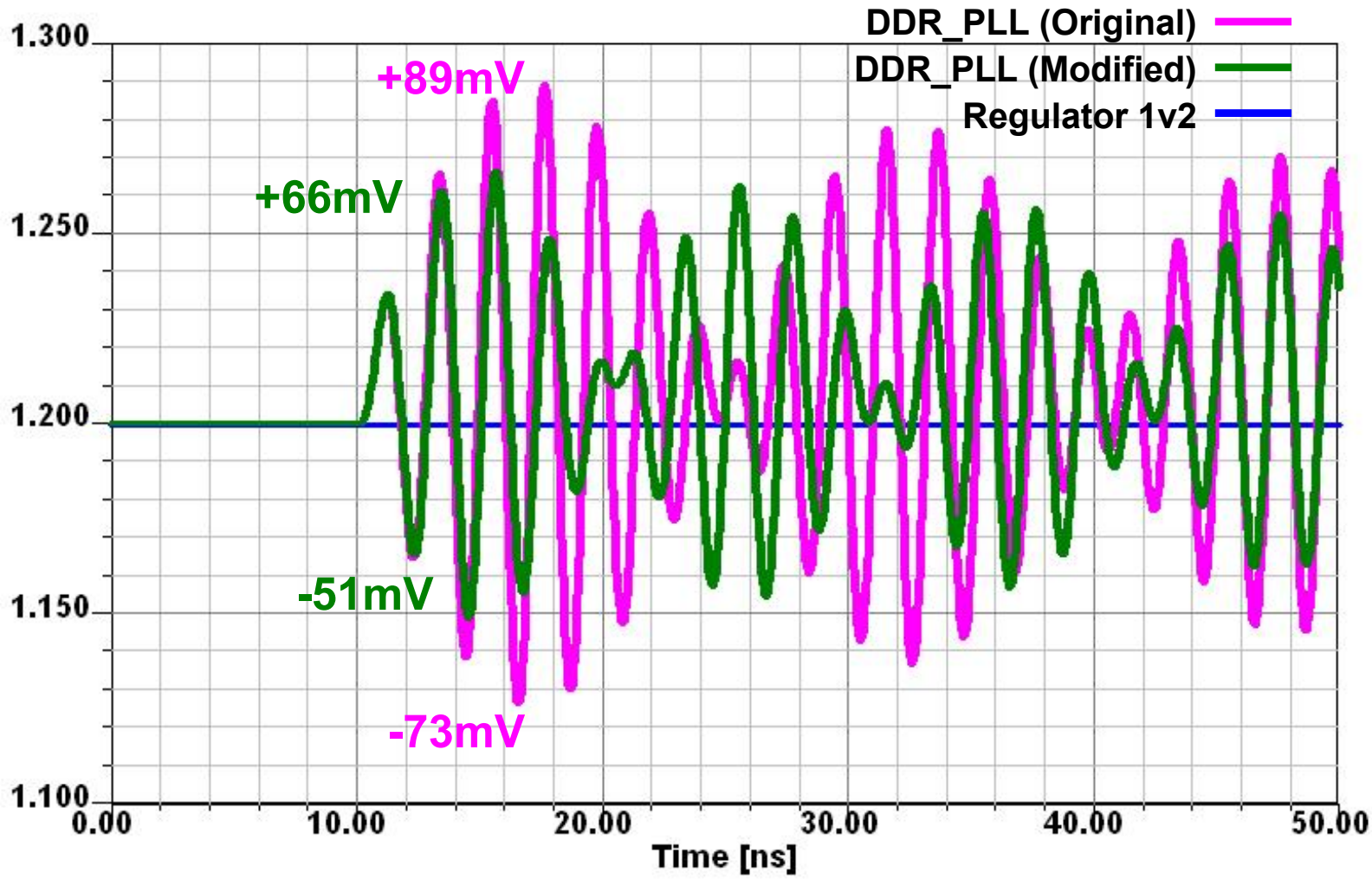
- There are no signals in the P/G loop of this case (between Layer3 and Bottom), so the effect is less.



VCC12A_DDR_PLL is affected by VDD18_DDR at Layer6 (1/2)



VCC12A_DDR_PLL is affected by VDD18_DDR at Layer6 (2/2)



The coupling noise can be reduced around 20%~30%

Agenda

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類別	學經歷條件
Analog IC Designer	對ADC、DAC、CODEC、PCI-EX、USB、LVDS、SATA、Power Management、PLL設計有興趣者
Memory Designer	對SRAM or ROM電路設計有興趣者
IO Circuit Design Engineer	對Standard cell library電路設計、Memory/Library IP驗證流程有興趣者
Display IC Designer	對Display相關的high speed LVDS、 DisplayPort、PLL、CDR 等系統結構有興趣者
HSIO Digital Designer	對USB、PCIe、SATA控制器數位IC設計有興趣者
Verification Engineer	對IP Verifcaiton, System Verification, Verification Methodology, Verification Flow有興趣者
Digital Designer	熟 verilog, 對數位IC設計有興趣者
CAD Engineer	對VLSI Physical Design流程、Placement、Clock Tree Synthesis、Routing、Power Integrity有興趣者

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- 人際關係
  - 表達方式 (同理心) – 故事
  - 讚美 (感恩心)
  - 幫助他人 (熱心)
- 忍受挫折的能力
- 持續學習與創新
- **Jack Welch**
  - Over delivery
  - Do what you like (Like what you do?)


Thank You