



HowardDigital.com

Golden Gate Bridge in San Francisco



Wakato Bridge in Kita-Kyushu

Outline

- ① **Kyushu Institute of Technology**
- ② **Power-Aware Testing: The Next Stage**

Outline

- ① Kyushu Institute of Technology
- ② Power-Aware Testing: The Next Stage

Outline

① Kyushu Institute of Technology

② Power-Aware Testing: The Next Stage

Something about Kyushu (九州)



Something about Kyushu (九州)

九州的溫泉



黑川溫泉

Something about Kyushu (九州)

九州的美食



河豚料理

Something about Kyushu (九州)

九州的汽車產業



年產150萬輛

Something about Kyushu (九州)

九州の半導體産業



又稱矽島，產能為日本的1/3

Kyushu Institute of Technology (九州工業大學)

技術に堪能なる仕君子

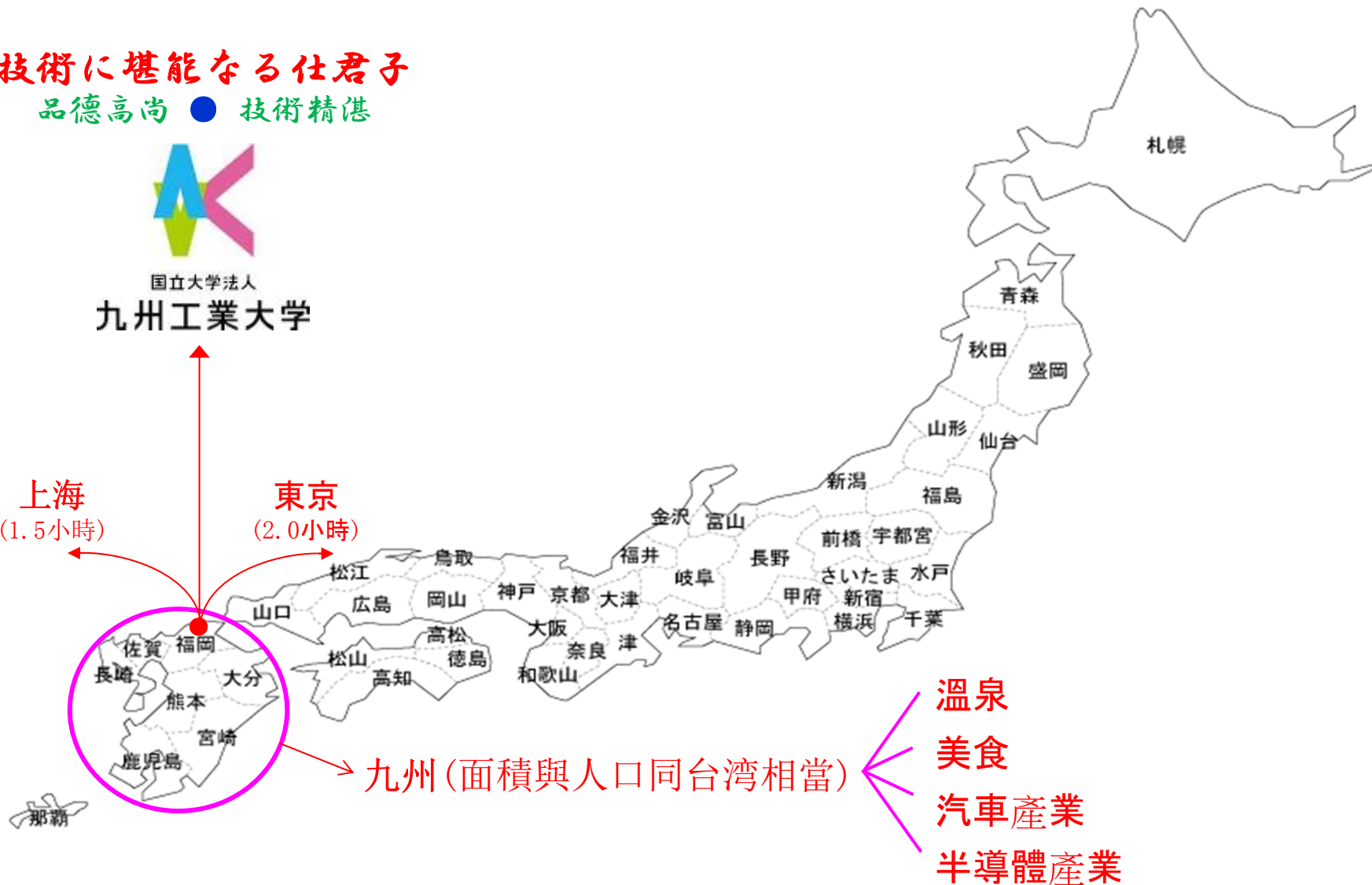
品德高尚 ● 技術精湛



国立大学法人
九州工業大学

上海
(1.5小時)

東京
(2.0小時)



九州(面積與人口同台灣相當)

温泉
美食
汽車產業
半導體產業

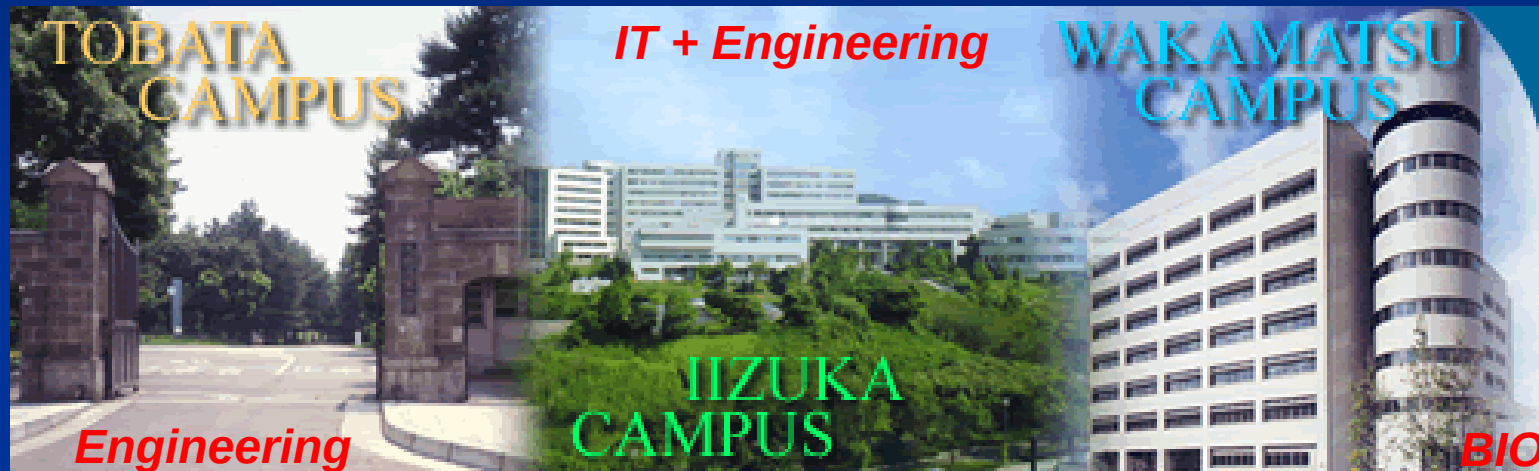
Kyushu Institute of Technology (九州工業大學)





九州工業大學

Kyushu Institute of Technology



- 1909年 私立「明治專門學校」成立，為日本最早的工科院校。
- 1921年 移交給政府，成為國立大學。
- 1949年 更名為「九州工業大學」。
- 1986年 在原有的「工學院」之外，成立日本第一個「資訊工學院」。
- 2000年 成立「生命體研究院」，進行生物技術的教育與研究。
- 2009年 建校100周年。

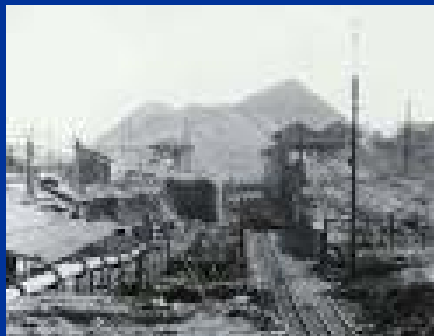
→最有名校友：藤田哲也（芝加哥大學教授），Fujita-Scale發明人。

創立者



安川敬一郎

明治礦業



安川電機



世界最大工業用機器人廠家

九州工業大學



日本歷史最久的工業大學

筑豊の炭鉱王



伊藤伝右衛門



牟田炭坑



柳原白蓮



皇族，大正3美人之一，詩人

嘉穂劇場



西日本最大の大衆劇場



国立大学法人
九州工業大学

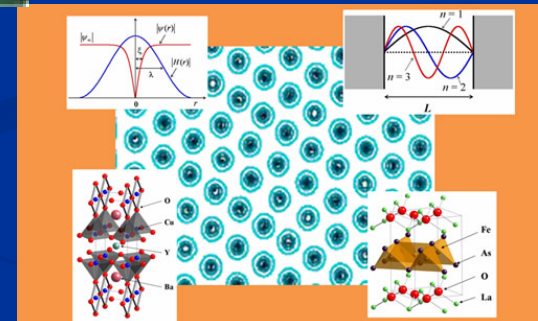
Kyushu Institute of Technology

Facilities - Tobata Campus 工學院（戸畑校區）



工學院 (戶畑校區)

- 智能機械工程系
機械工學
宇宙工學
智能控制
- 建設社會工程系
建築學
地域環境設計
都市再生設計
- 電氣電子工程系
電子系統
電氣能源
電子器件
- 應用化學工程系
- 物質工程系
- 綜合系統工程系





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九州工業大学

Kyushu Institute of Technology

Facilities - Iizuka Campus 資訊工學院 (飯塚校區)



資訊工學院（飯塚校區）

- 智能資訊工程系
- 電子資訊工程系
- 系統創成工程系
- 機械資訊工程
- 生命資訊工程系





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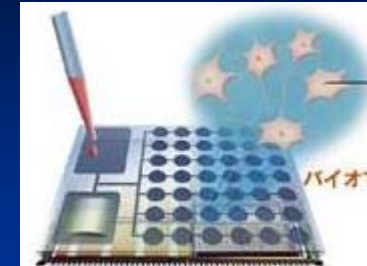
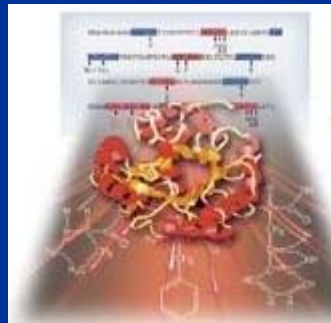
Kyushu Institute of Technology

Facilities - Wakamatsu Campus 生命體研究院 (若松校區)



生命體研究院 (若松校區)

- 生體機能研究系
- 脳資訊研究系





九州工業大學

Kyushu Institute of Technology

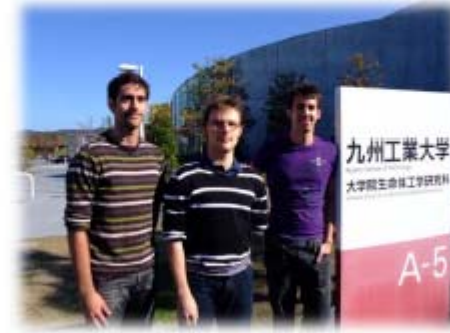
- 學生總數 6035（本科生 4296，研究生 1739）
- 留學生總數 217（來自 27 個國家）
- 教職員總數 559（教授 134，副教授 147，助教 69）
- 年度預算總額 109 億日元
- 資訊工學部全部通過JABEE認證
- 就職支援度第 1 位
- 就職率第 7 位
- 地域貢獻度第 4 位（國立大學中最高）
- 大學創辦企業數第 7 位
- 環保貢獻度第 9 位
- 專利數第 16 位（國立大學中最高）



国立大学法人
九州工業大学

Kyushu Institute of Technology

Student Life



九州工業大學歡迎您

Power-Aware Testing

The Next Stage



Test

Power



Xiaoqing Wen
Kyushu Institute of Technology

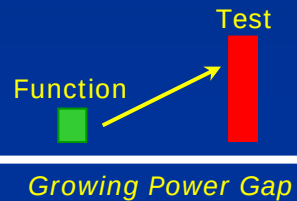


High Performance

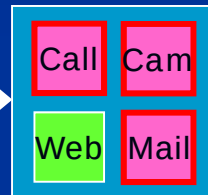
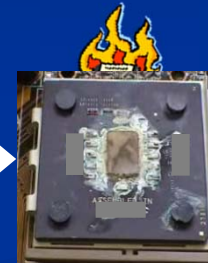
Successful
LSI
Product

Low Power

Function-Mode

Low Functional Power
(Wide Use of PMS)

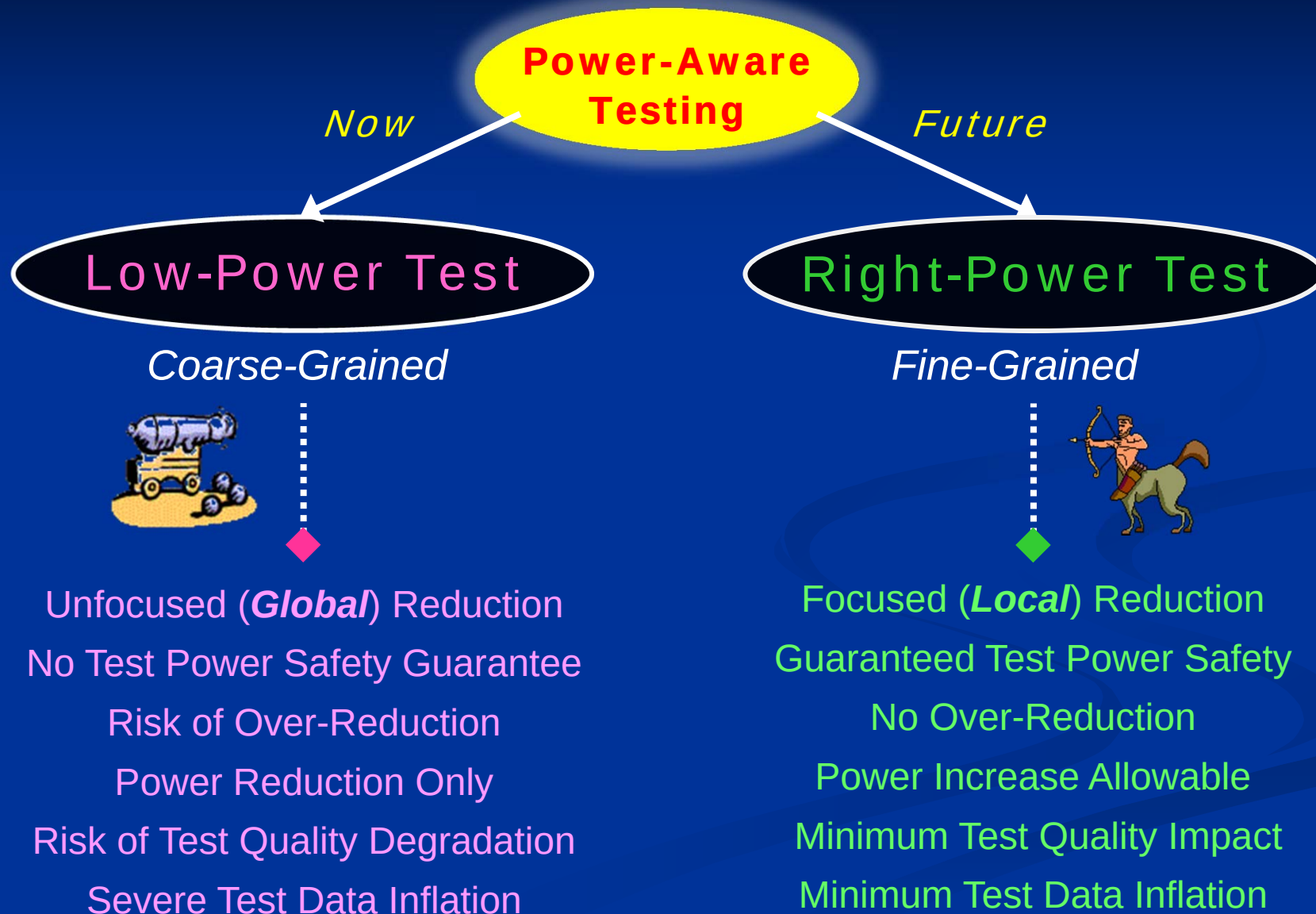
Test-Mode

High Test Power
(Needs to Handle PMS)Excessive Heat • Timing Failures
Higher Test Complexity due to PMS

Test Crisis

(Damage / Low Yield / High Cost)

Low
Power
DesignPower
Aware
Test



FYI

**2003 Most Significant Paper Award
@ International Test Conference 2013**

A Case Study of IR-Drop in Structural At-Speed Testing

J. Saxena, K. Butler, V. Jayaram, S. Kundu, N. Avind, P. Sreeprakash
Texas Instruments

M. Hachinger
Siemens

*The first paper that has shown the test power issue is real
and that test data manipulation can indeed reduce test power.*

Citations = 26.7 / year
(The famous FAN Paper: Citations = 24.5 / year)

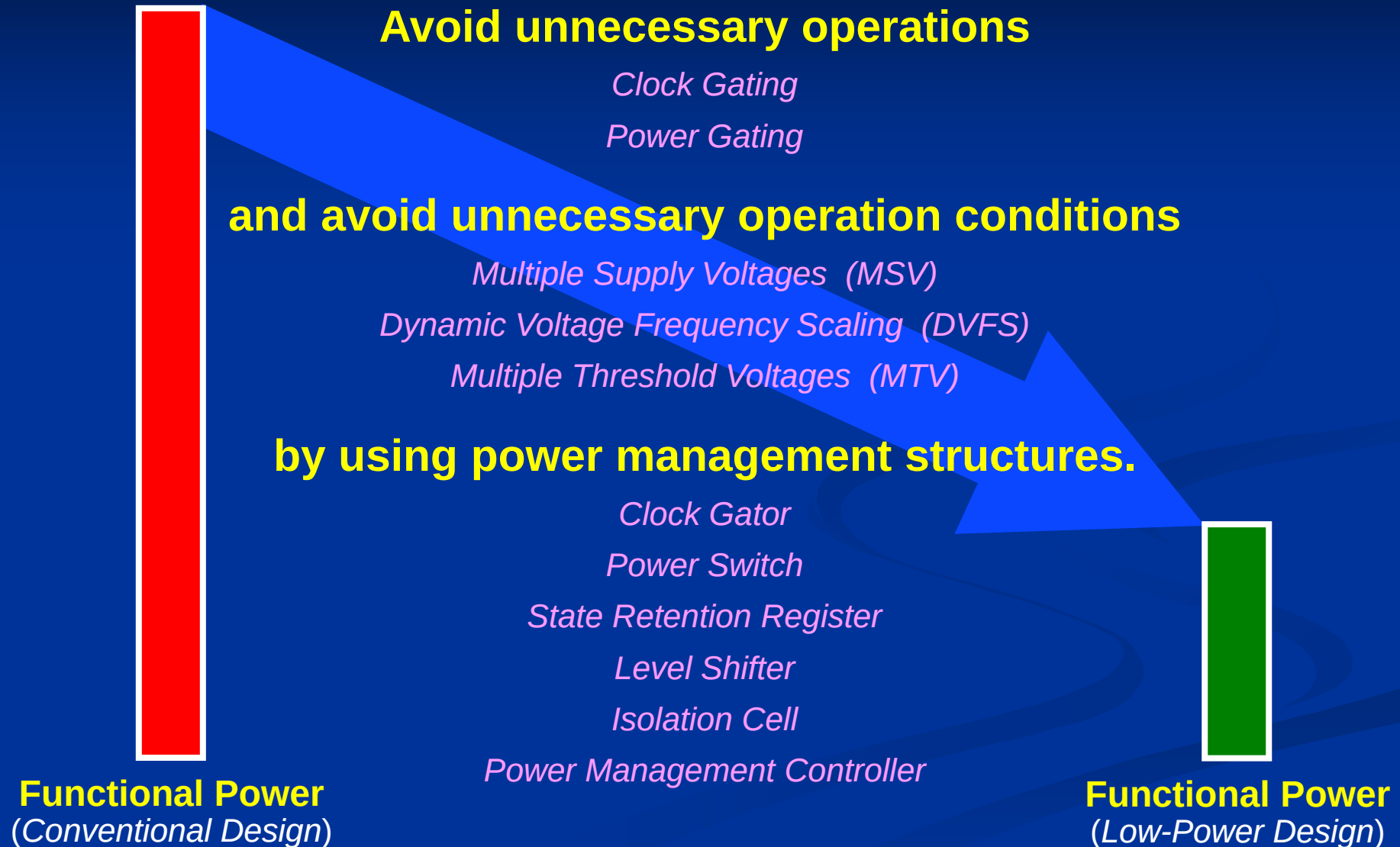
Outline

- ① **Power: Excitement for Design Engineers**
- ② **Power: Headach for Test Engineers**
- ③ **Test Power Analysis**
- ④ **Test Power Reduction**
- ⑤ **Next Stage and New Opportunities**

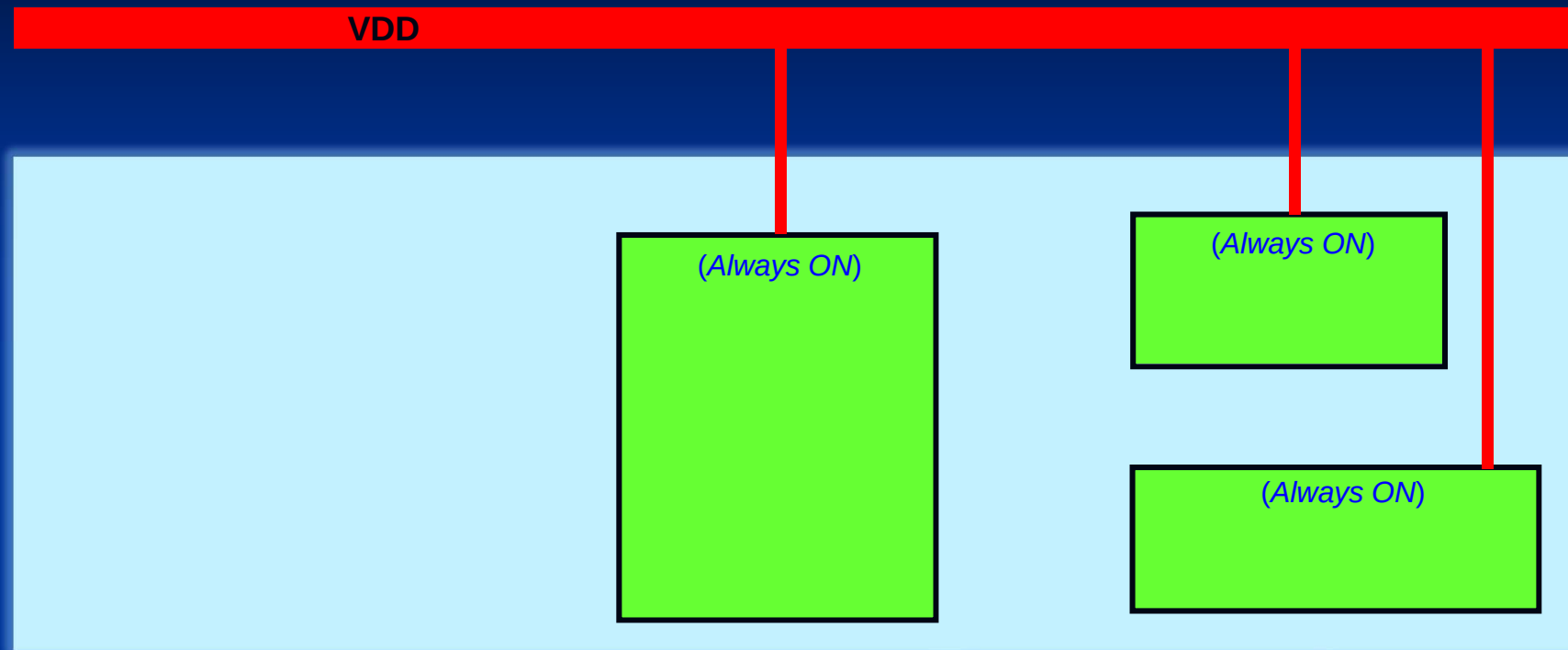
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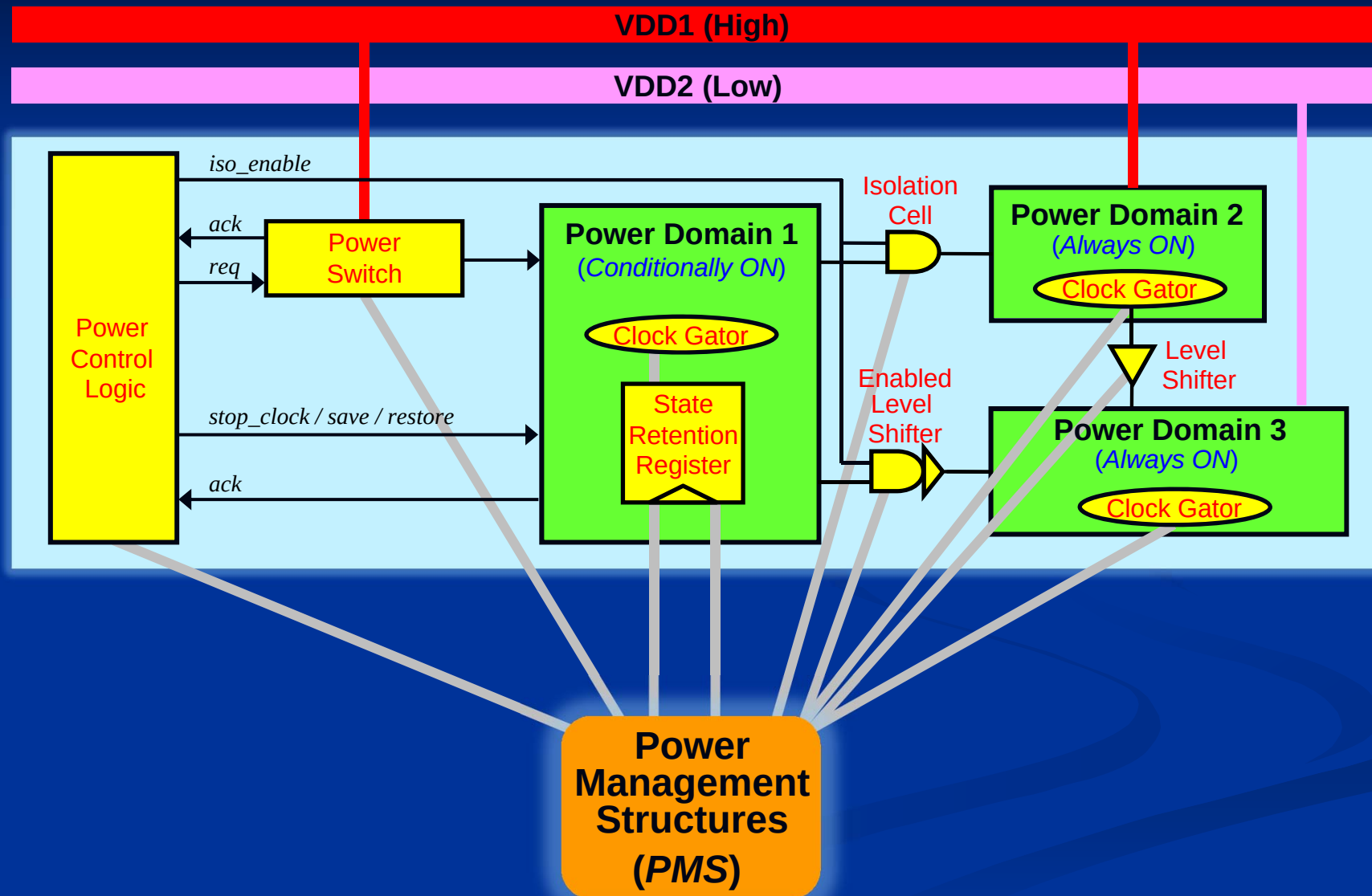
Design Engineers Love to Reduce Power



Conventional Design



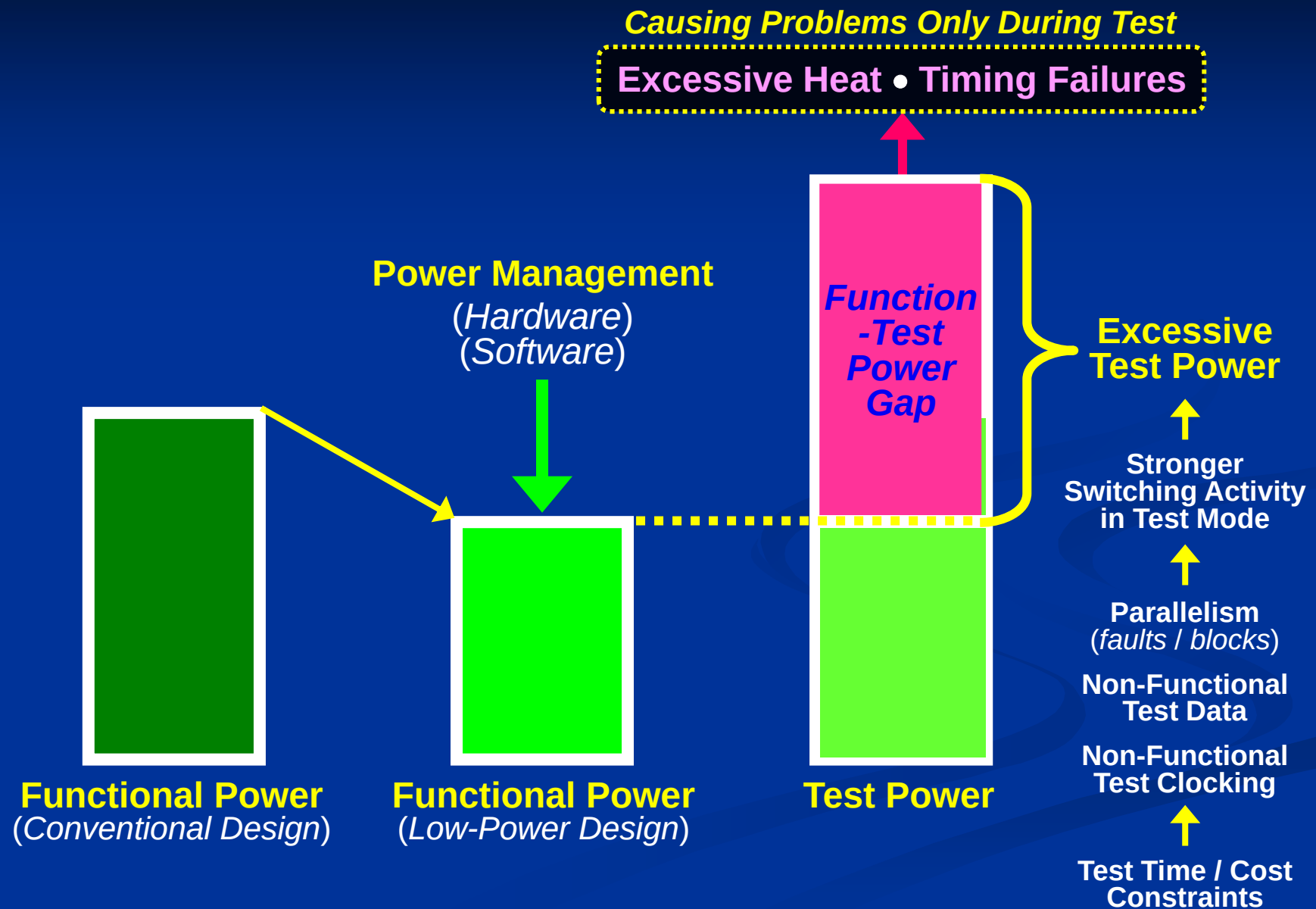
Low-Power Design



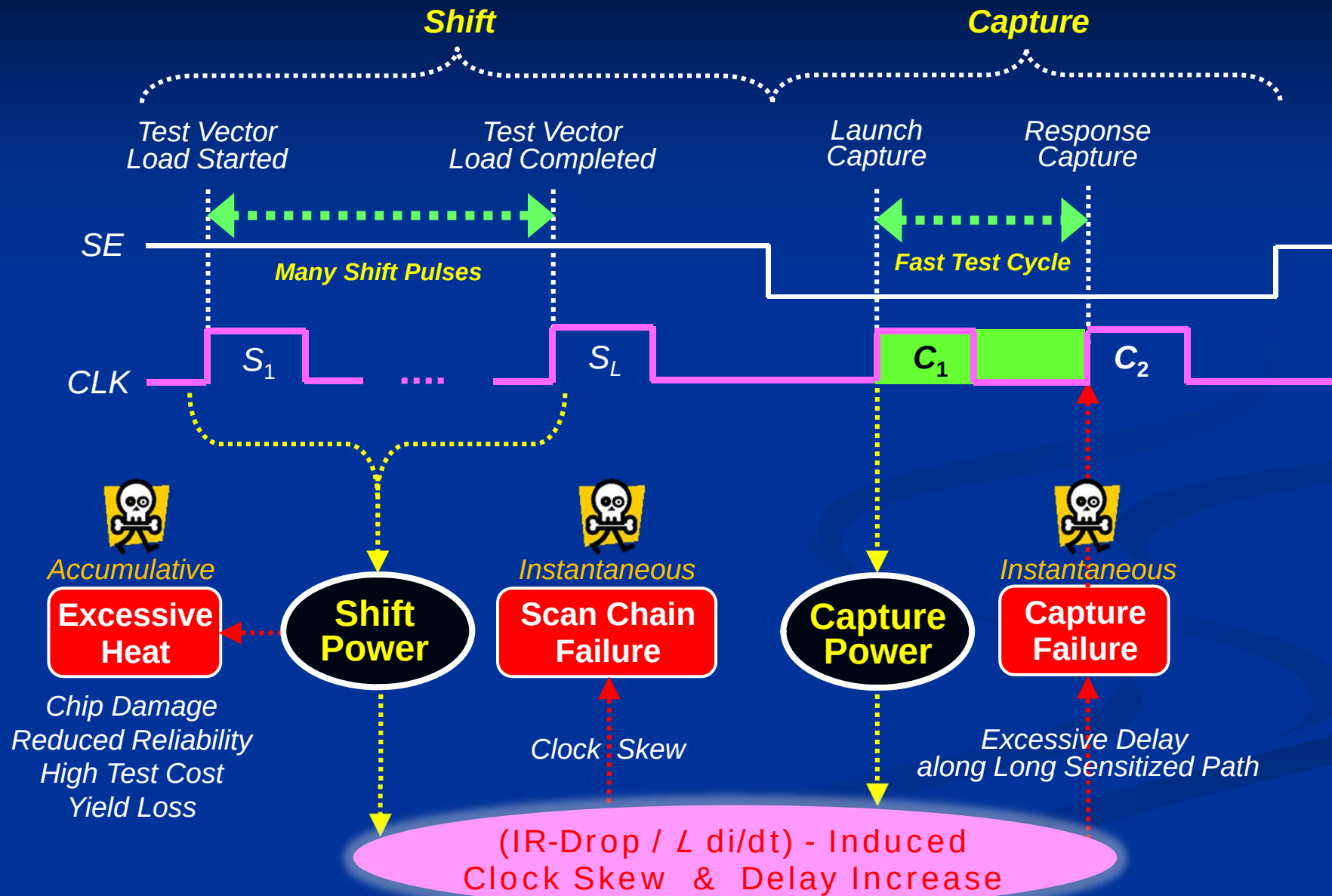
Outline

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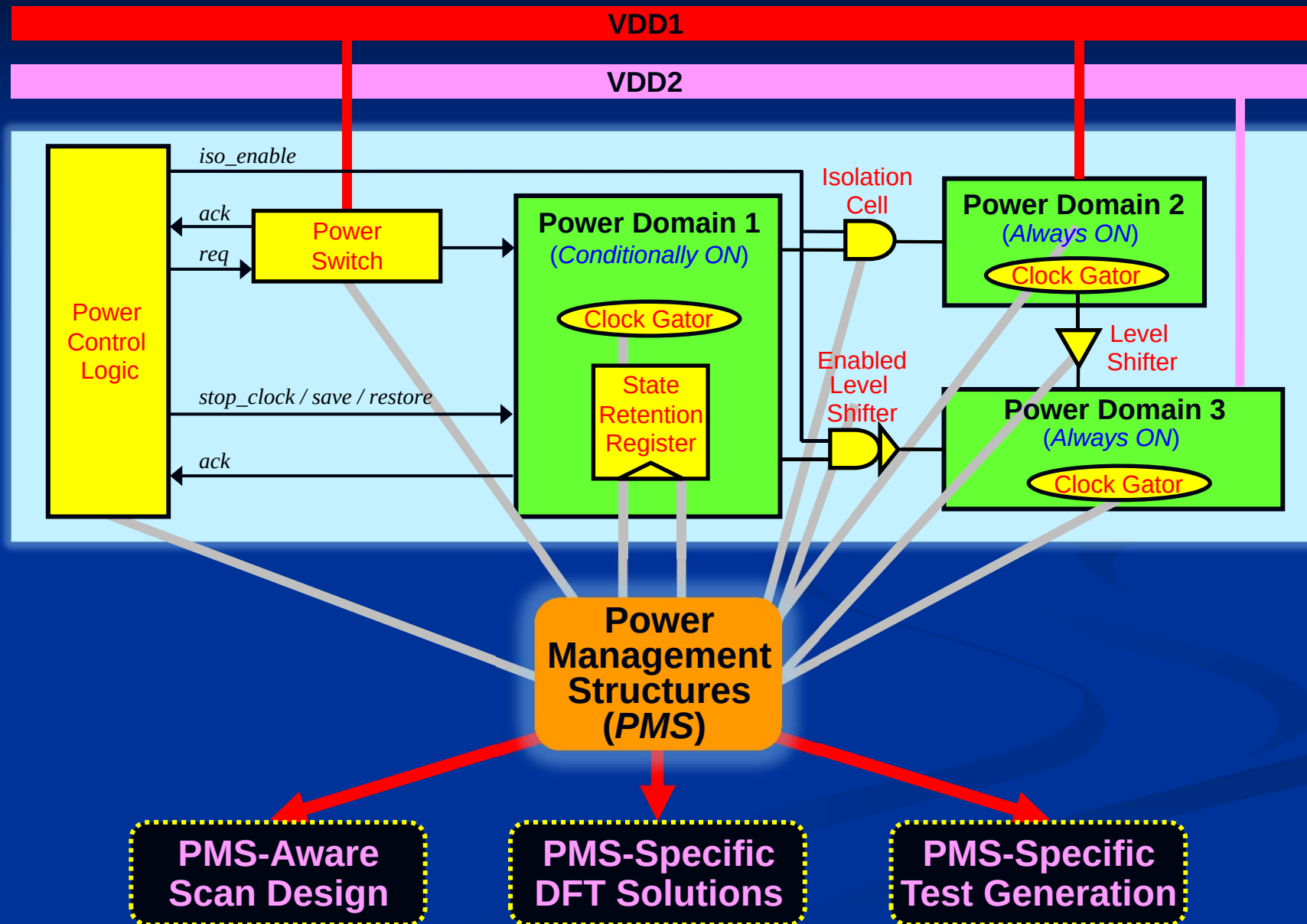
Widening Function-Test Power Gap



Impact of Test Power in At-Speed Scan Testing (LOC)



Power Management Structures Add to Test Complexity



Build Test Infrastructure



In the Old Days ...

- Scan Design
- Test Compression / BIST
- Testability Enhancement with TPI



Nowadays ...

- MSV-Aware Scan Design / Power-Gating-Aware Scan Design
- Low-Power Test Compression / Low-Power BIST
- Testability Enhancement with TPI and for PMS (*especially, power switches*)
- Design for Shift Power Reduction / Design for Capture Power Reduction

Generate Test Data



In the Old Days ...

- Conventional ATPG



Nowadays ...

Scan Test Power Reduction

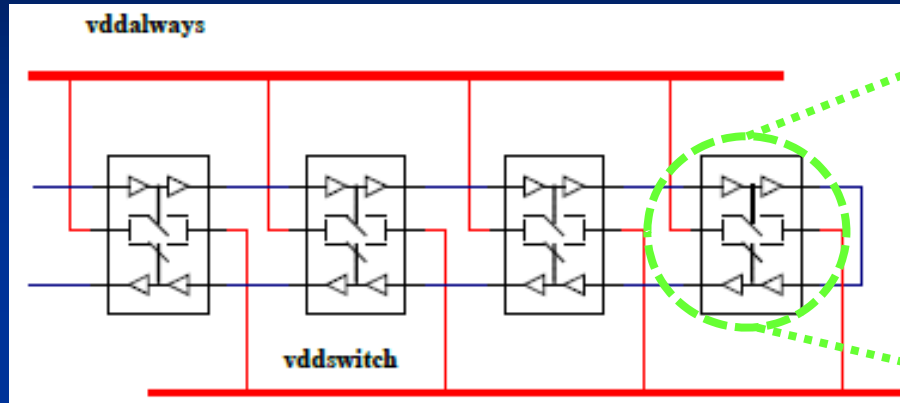
- Test Power Analysis
- Test Power Reduction (*low-shift-power ATPG / low-capture-power ATPG*)

Power-Management-Specific Concerns

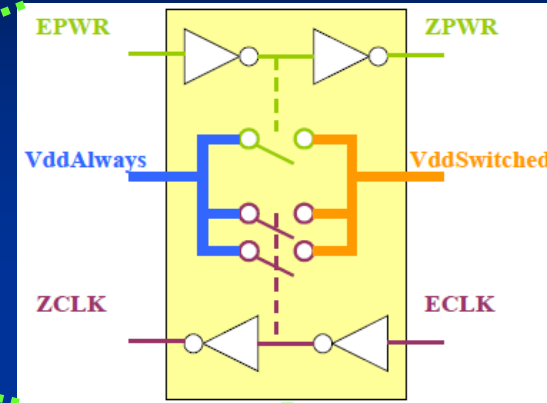
- System-Level Power-Aware Scheduling due to Limited Power Budget
- Test Generation for MSV
- Test Generation for Power Management Structures

An Example: DFT for a Complex Power Switch

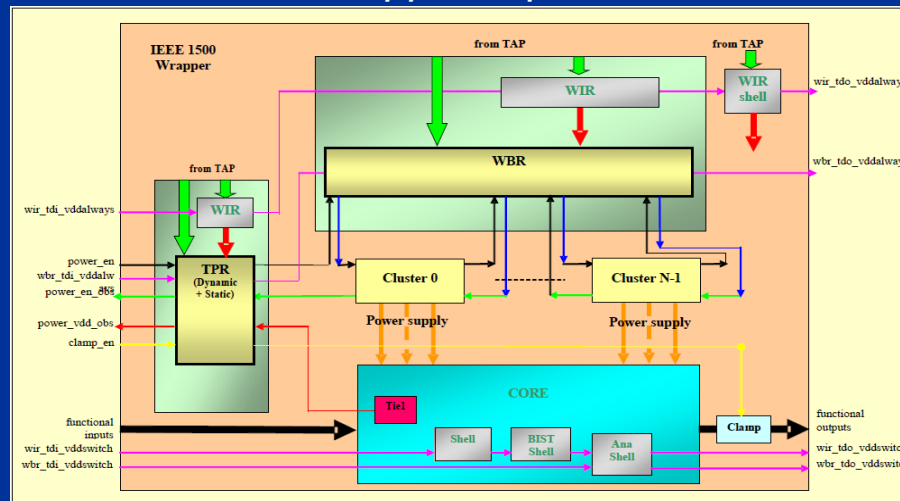
Micro Power Switch Chain
for containing rush current



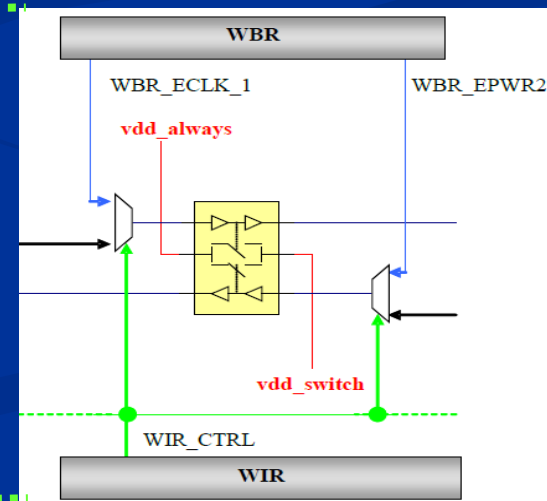
One Power Switch
before DFT



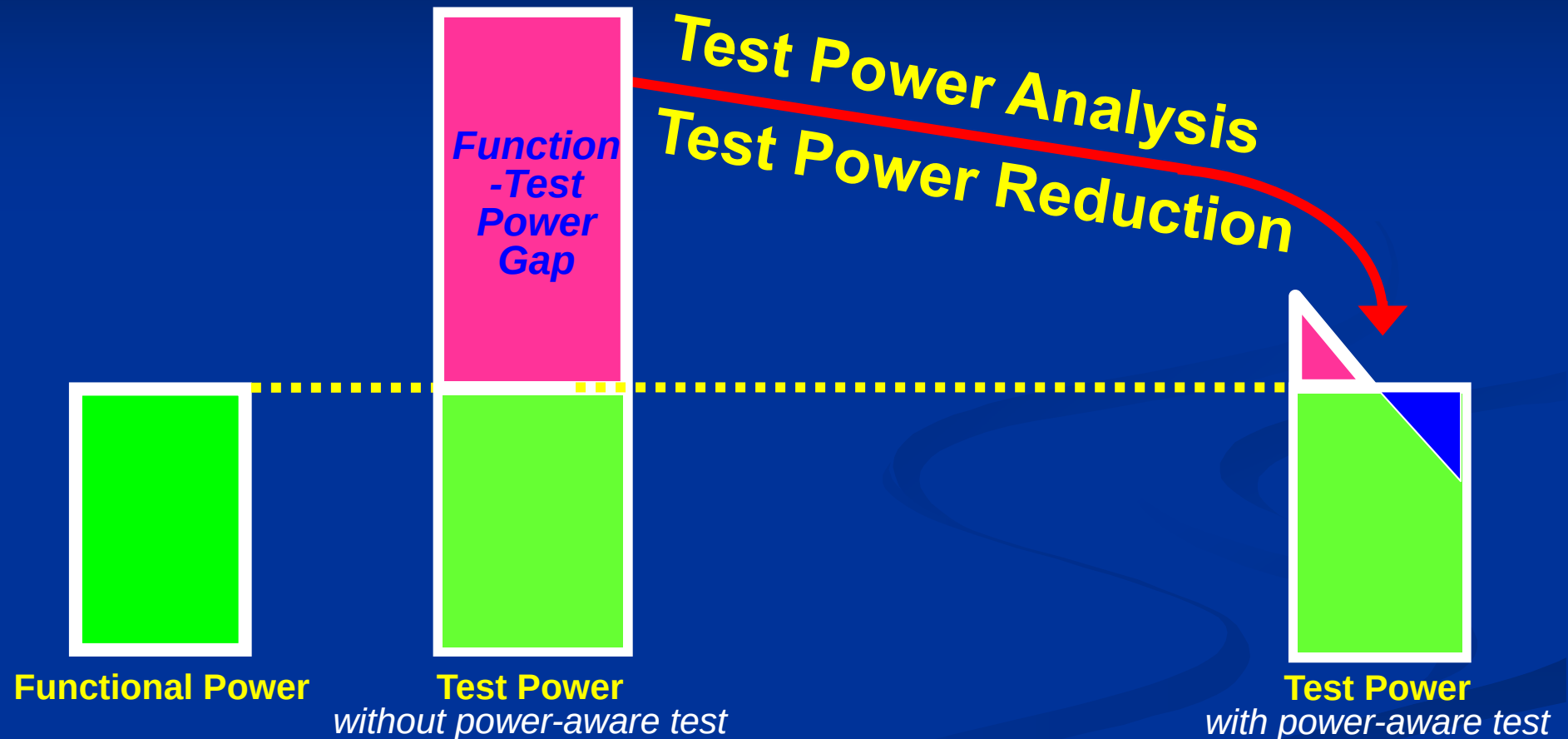
Micro Power Switch Chain
with test wrapper implementation



One Power Switch
after DFT



Basic Tasks in Handling Function-Test Power Gap



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Ideal vs. Reality

Switching Activity

Ideal

Reality

- Accurate but costly.
- OK for sign-off but expensive for use in DFT / ATPG.

- Fast and accurate-enough approximation needed.
- Gate-level metric preferred.

→ **Global**
→ **Local**

Temp.
Analysis

IR-Drop
Analysis + Delay
Analysis

Sensitization
Analysis

Excessive Heat

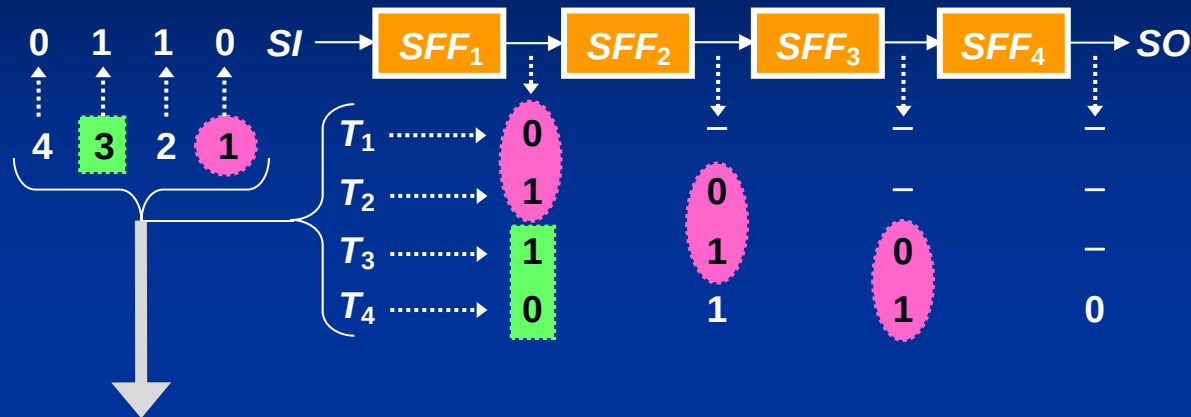


Excessive Delay along Sensitized Paths

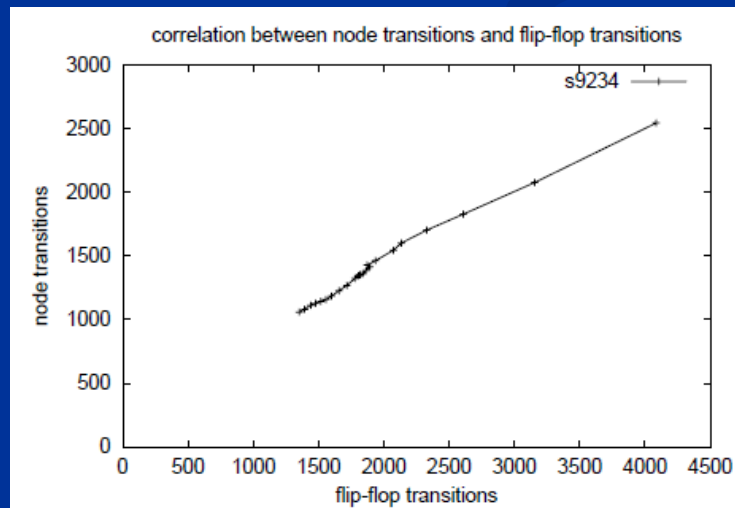


Global Shift Power Analysis: *Checking for Heat Issues*

Estimating Accumulate Impact of Shift Power



Weighted_Transitions = $\sum (\text{Scan_Chain_Length} - \text{Transition_Position})$

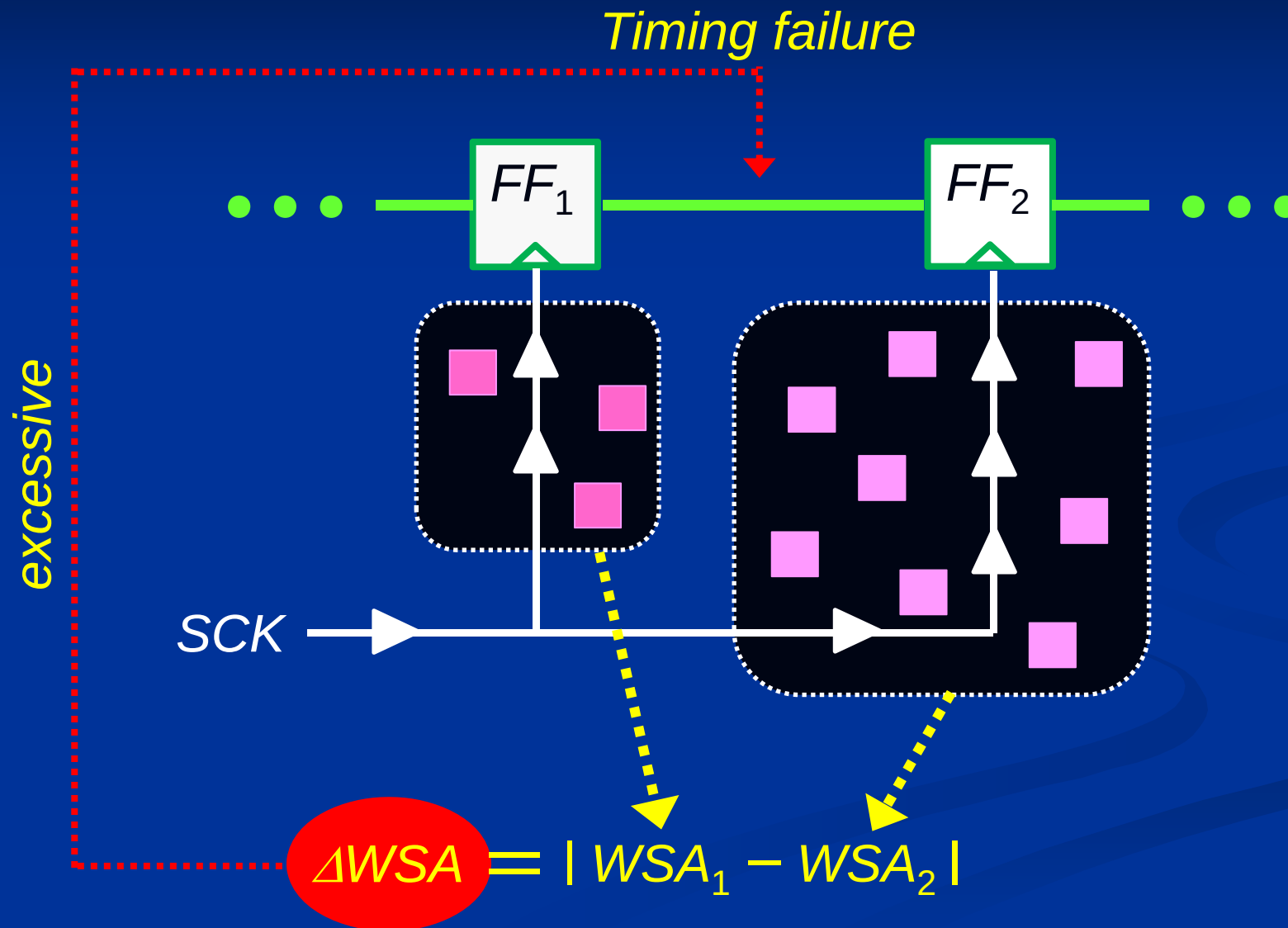


Switching in the CUT →

← Switching at FFs

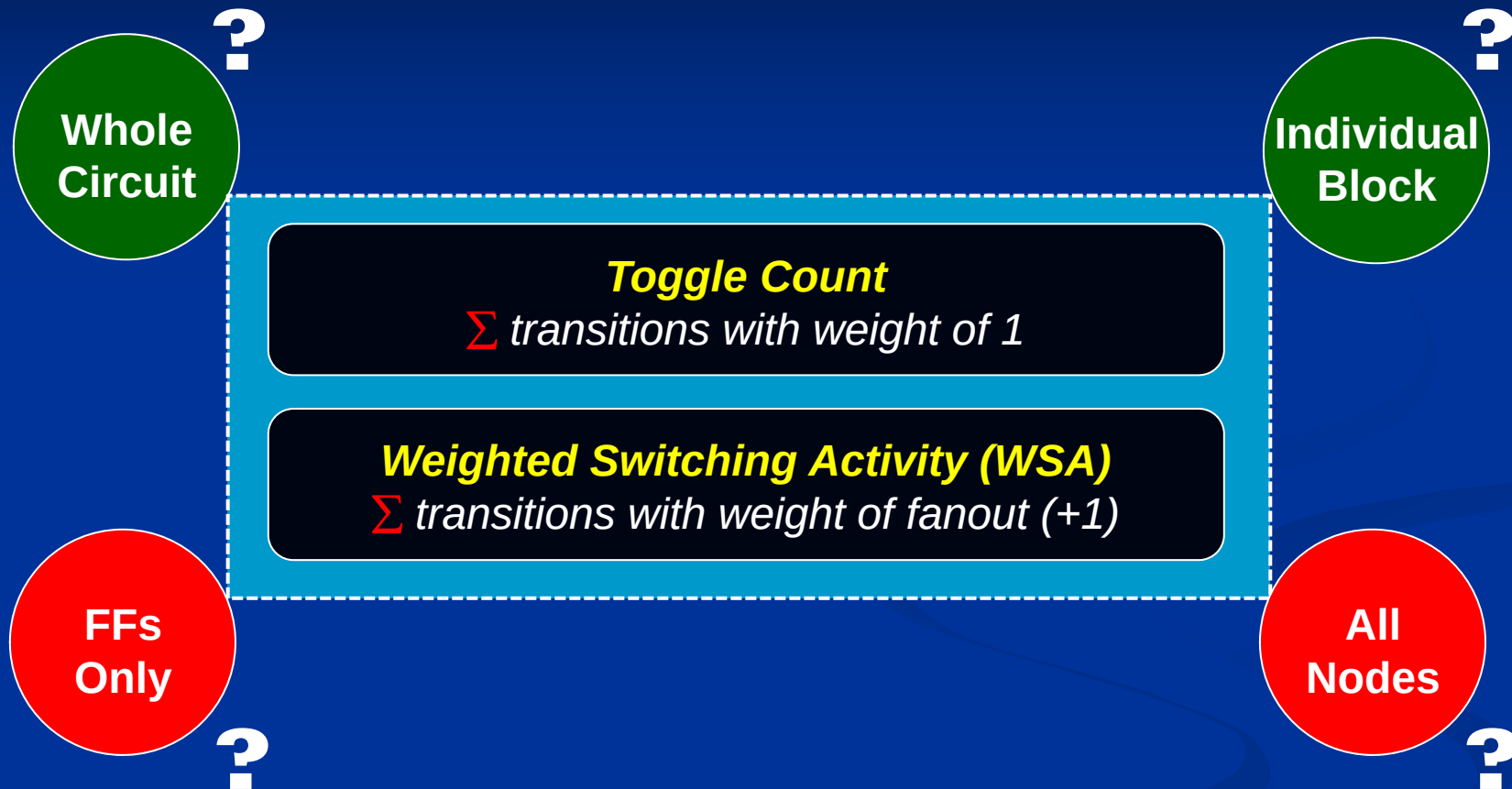
Local Shift Power Analysis: Checking for Timing Issues

Estimating Instantaneous Impact of Shift Power



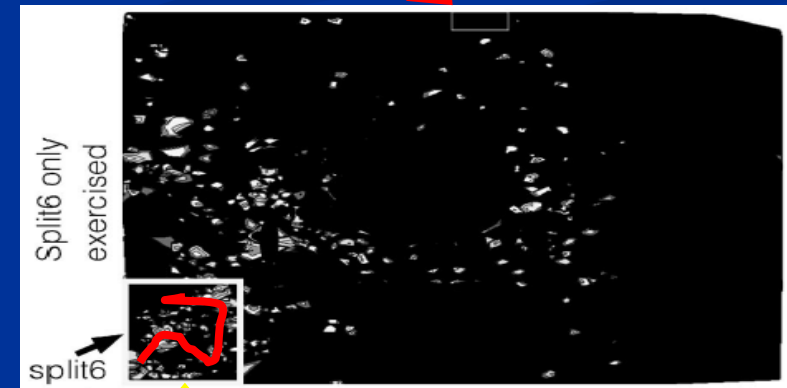
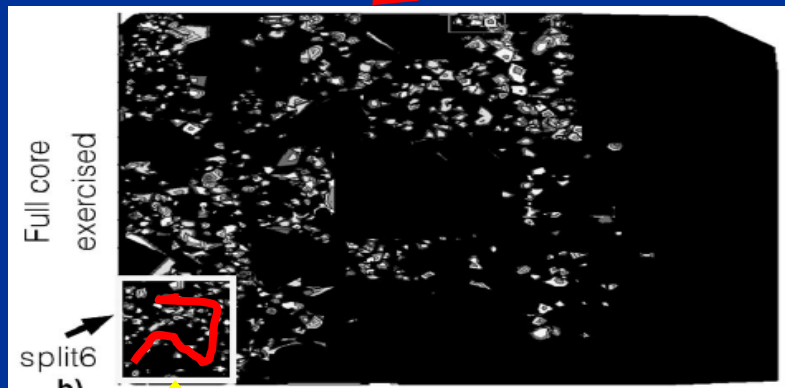
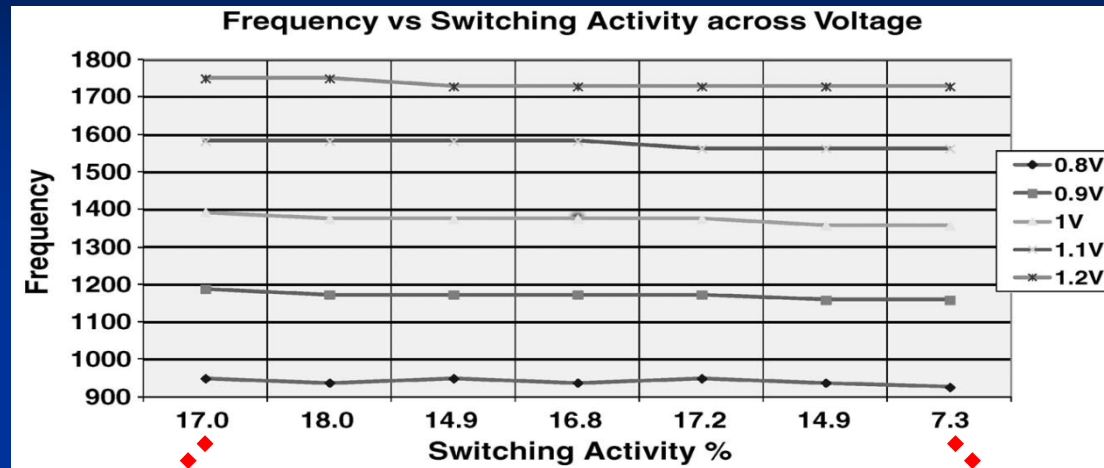
Global Capture Power Analysis: *Basics*

Capture Power



Global Capture Power Analysis: *Potential Problem*

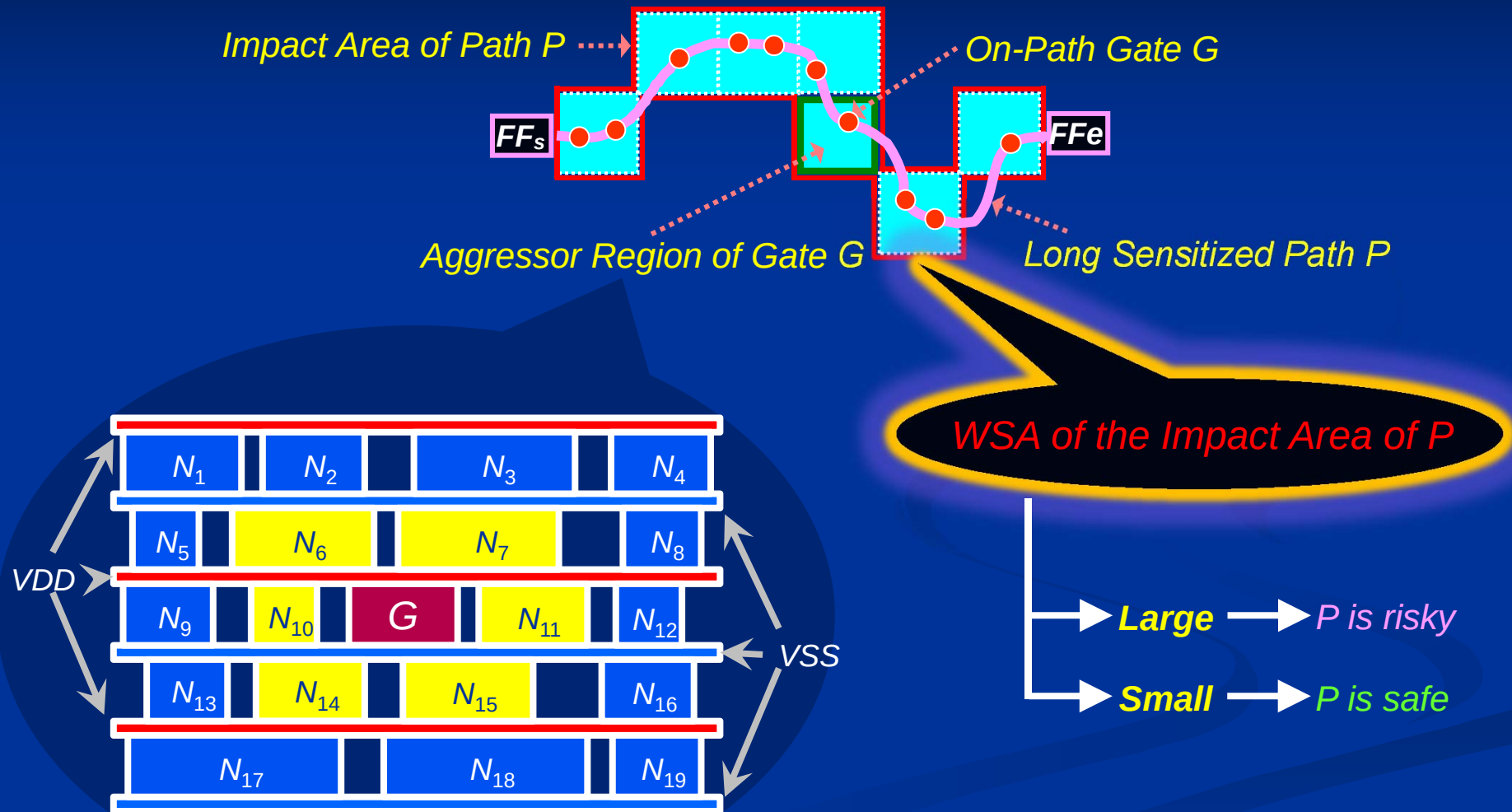
Low Correlation between Path Delay and Global SA



Maximum Frequency Determining Path

Local Capture Power Analysis: *More Accurate*

LSP (Long Sensitized Path) Based Analysis



Outline

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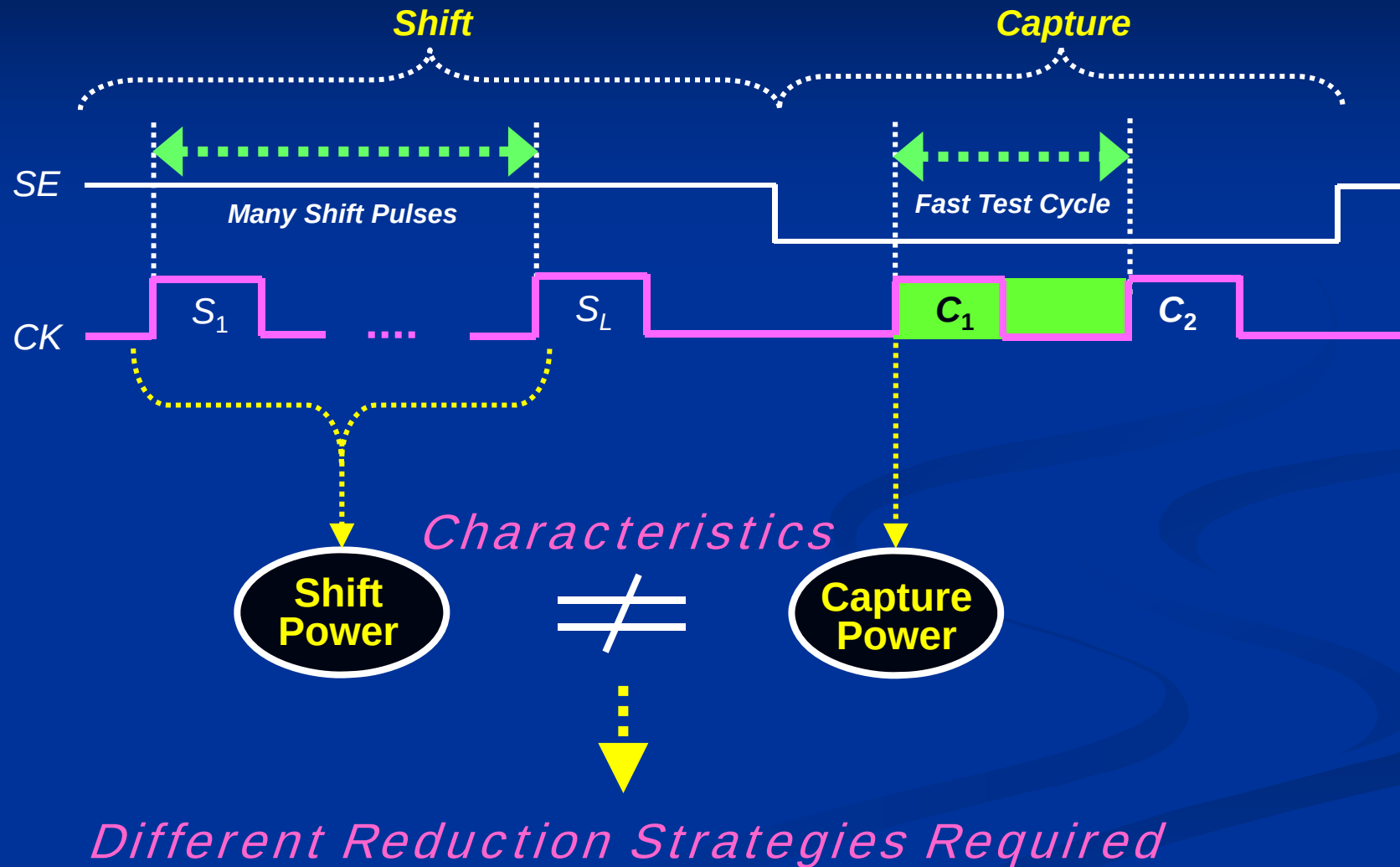
Basic Strategies

Shift Power Reduction

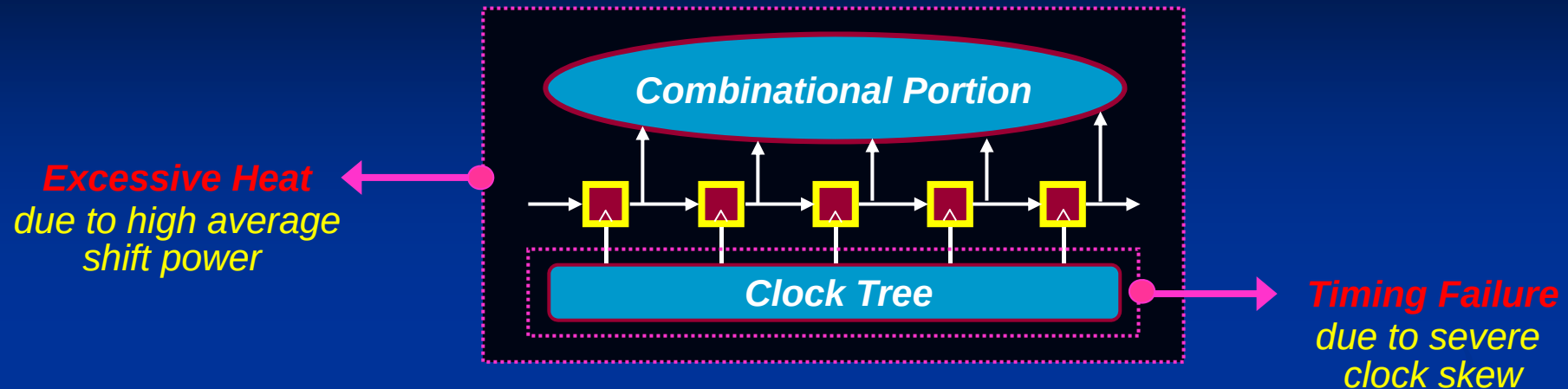
Capture Power Reduction

Basic Strategies

Different Characteristics of Shift and Capture Power

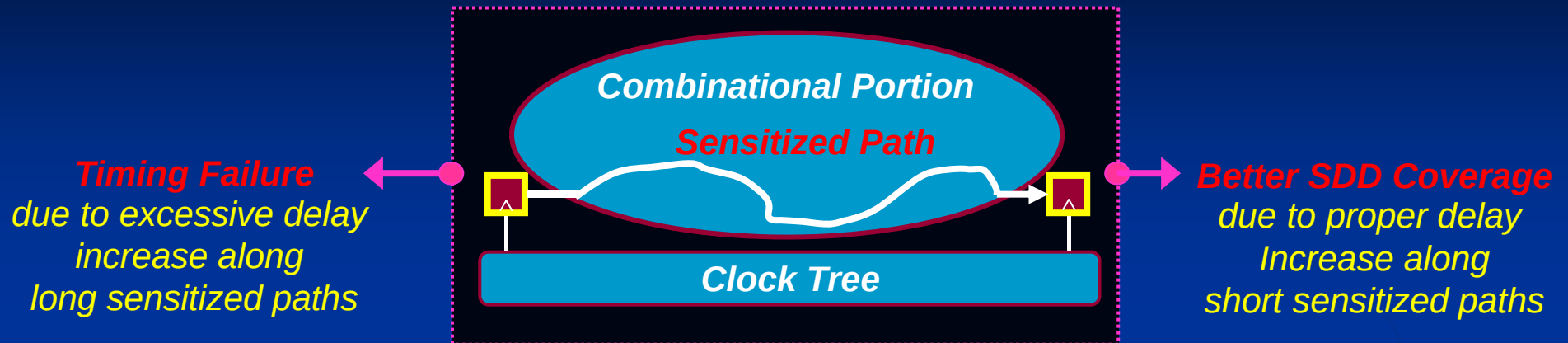


Characteristics of Shift Power



- ➔ *Shifting a test vector often causes heavy switching activity.*
-  ➔ *IR-drop is often worse in shift mode than in capture mode.*
- ➔ *All test vectors contributes to the shift power problem.*
- ➔ *Slowing down helps reduce heat impact but not clock skew.*
-  ➔ *Circuit / clock change has no impact on ATPG, time, size, and FC.*
- ➔ *Only scan chains need to be considered as sensitized paths.*

Characteristics of Capture Power



- Capture power impact only shows up at sensitized paths.
- Reducing capture power may be needed to avoid yield loss.
- Circuit / clock change may impact ATPG, time, size, and FC.



- Capture power depends on the content of a test vector.
- A small portion of test vectors suffers from excessive capture power.
- Increasing capture power may help to improve test quality.
- Functional power management circuitry helps reduce capture power.

Basic Strategies for Test Power Reduction

Type of Test Power Reduction Techniques $\begin{cases} \text{Soft:} & \text{Test Data Manipulation} \\ \text{Hard:} & \text{Circuit Modification} \end{cases}$

Effect

Soft—Soft—Soft

Soft
Global (Ave.) Shift Power Reduction

Soft
Local (Peak) Shift Power Reduction

Soft
Capture Power Reduction

- severe shortage of X-bits

Hard—Soft—Soft

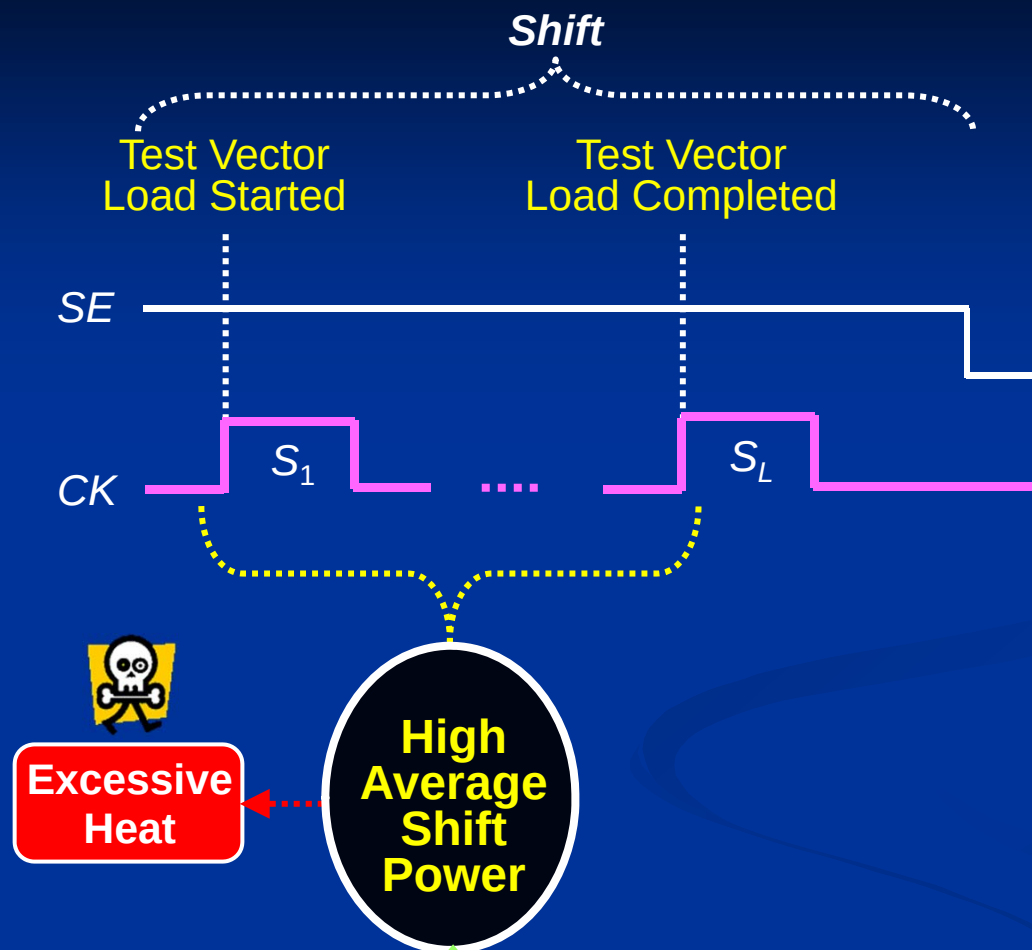
Hard
Global (Ave.) Shift Power Reduction ✓

Soft
Local (Peak) Shift Power Reduction

Soft
Capture Power Reduction ✓

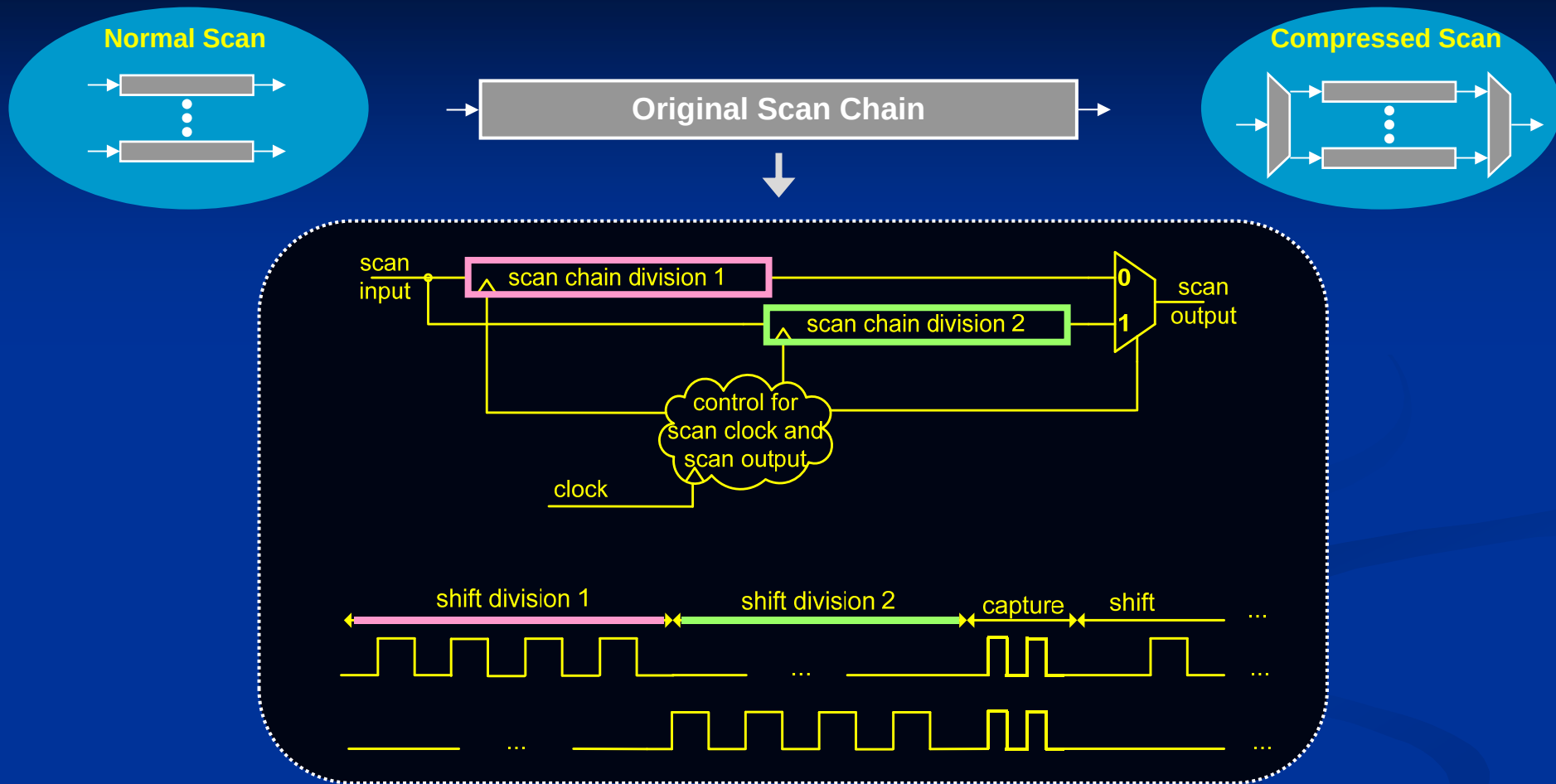
- predictable heat reduction
- low-overhead delay management
- focused delay management
- low test data inflation

Overhead

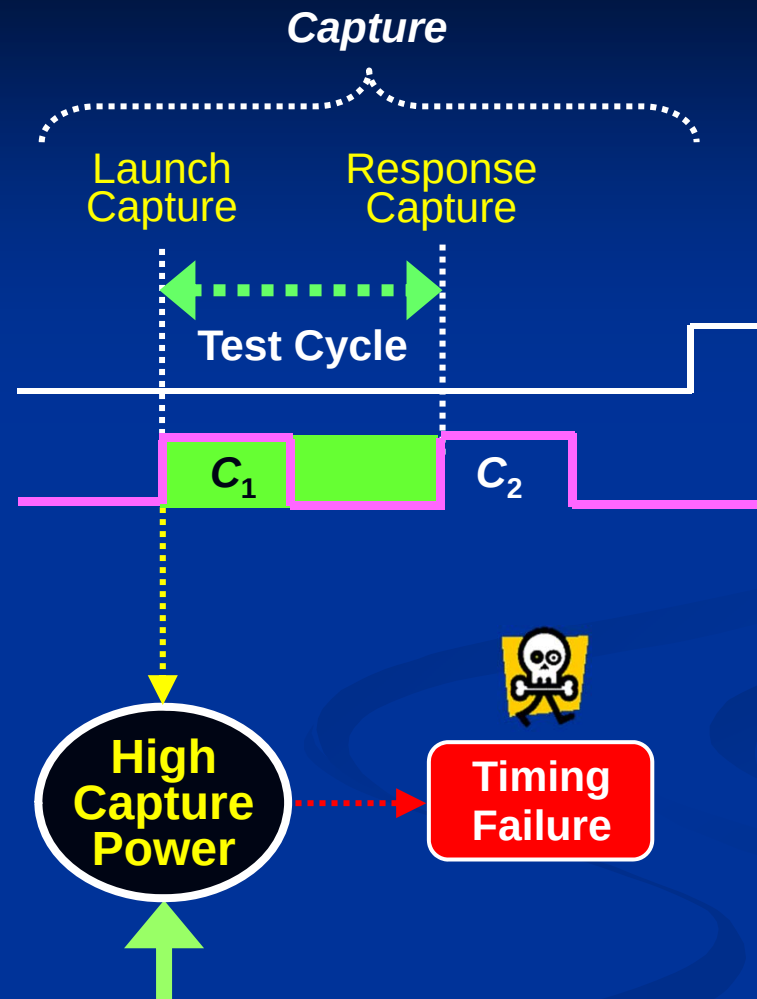


Ave. Shift Power Reduction

Scan Segmentation

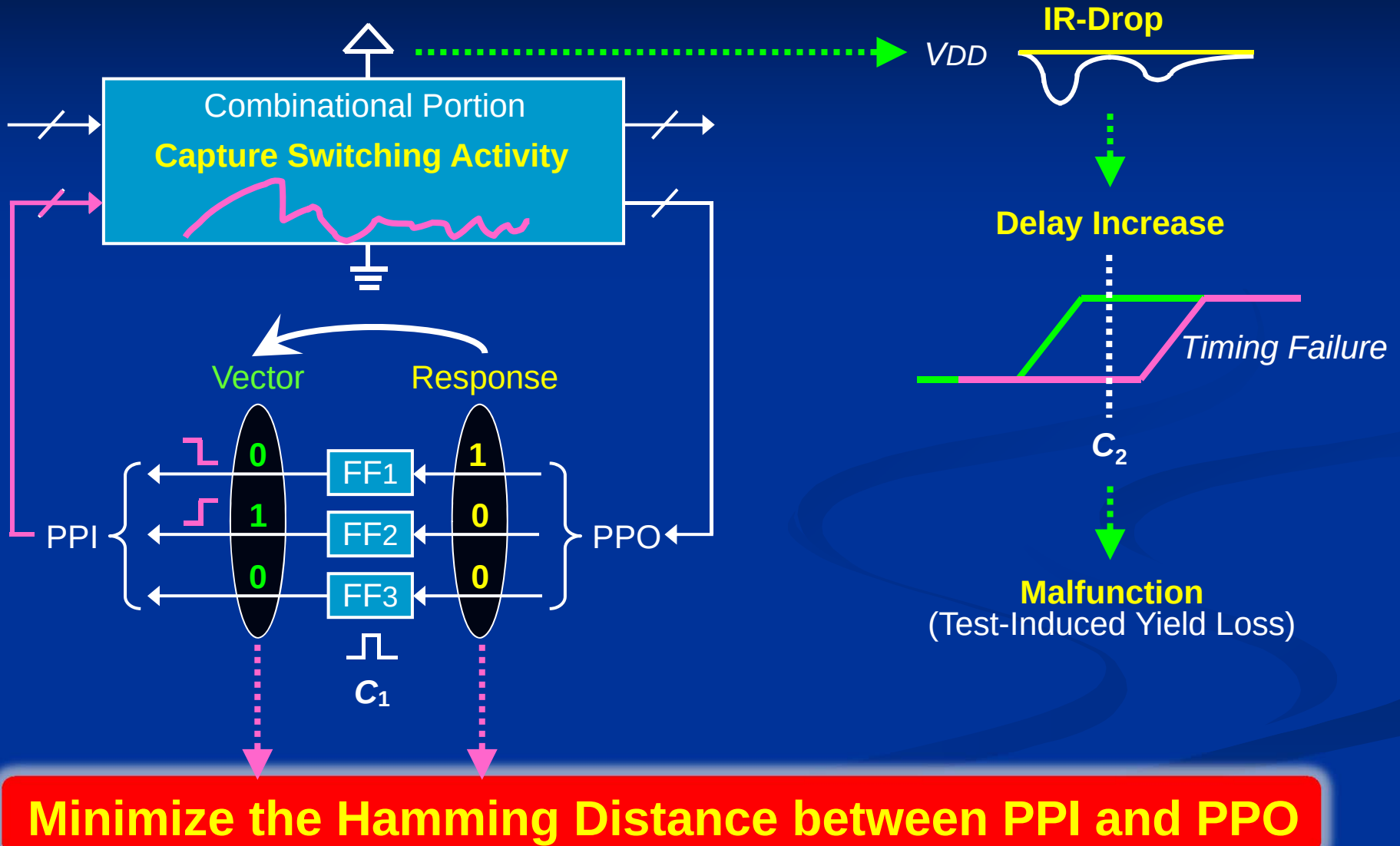


Predictable and data-independent shift (in & out) power reduction.
No change to ATPG and no increase in test application time.



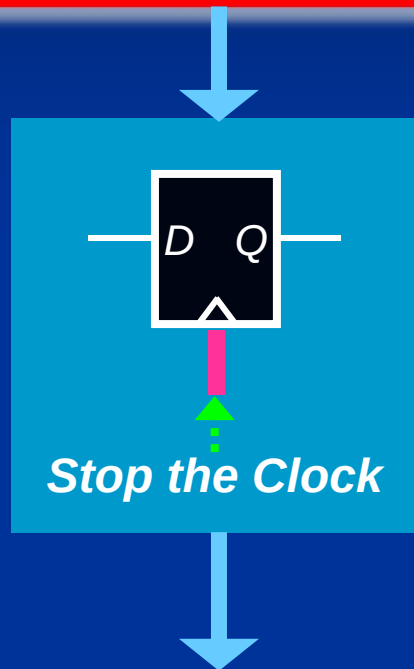
Capture Power Reduction

Capture Power Reduction: *Principle*



Capture Power Reduction: *Approaches*

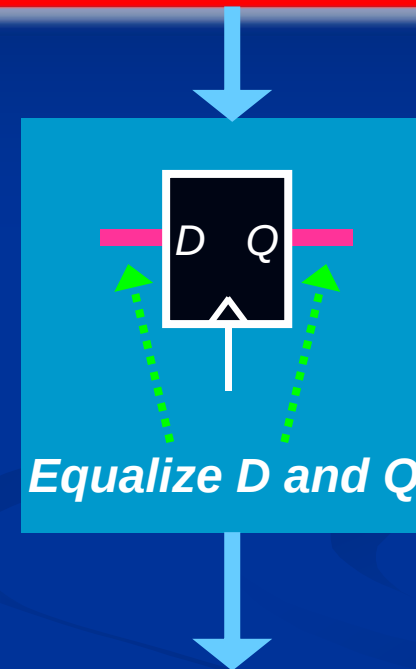
Reduce the Number of Simultaneously-Capturing FFs



Clock Control Modification

Test Vector Manipulation

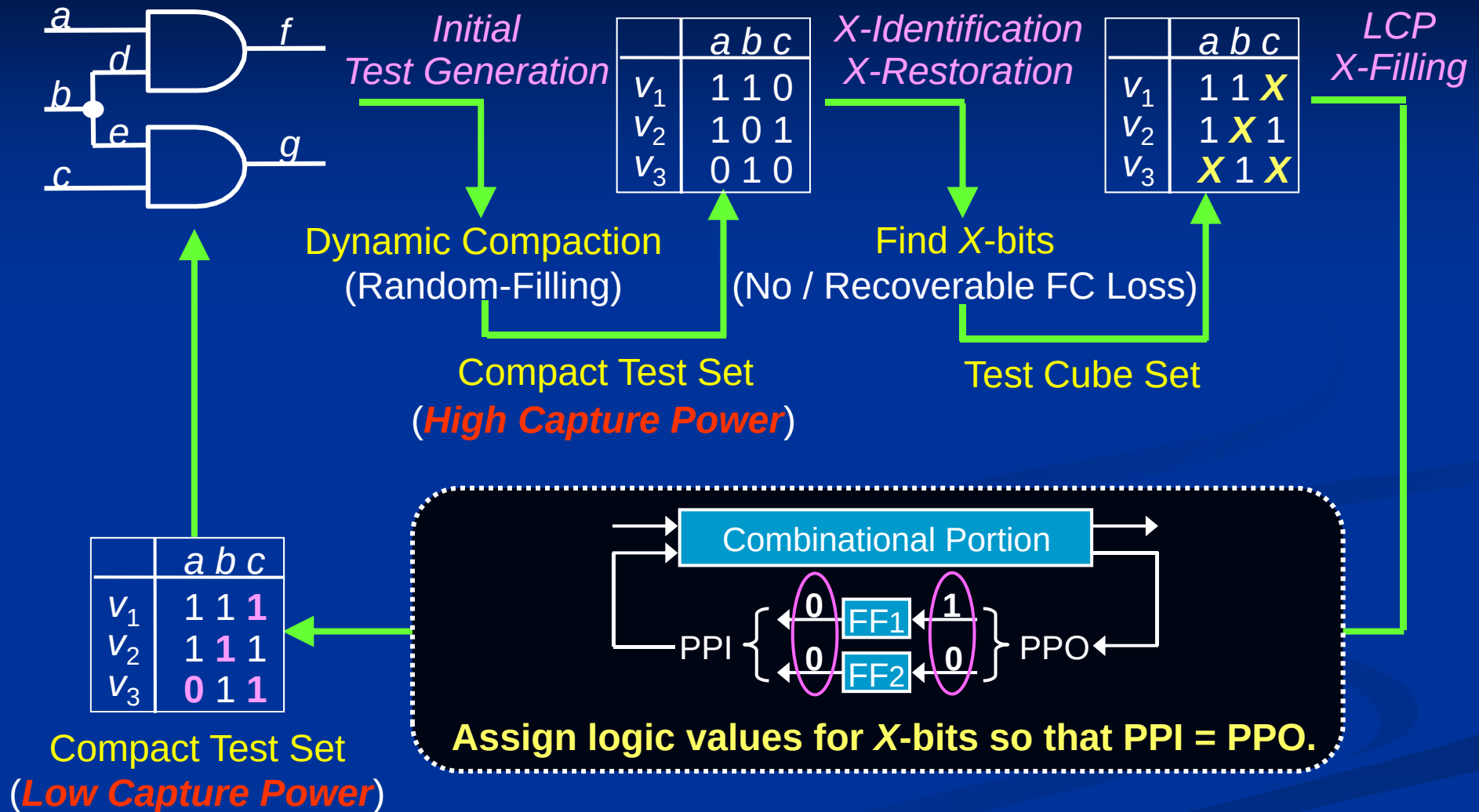
In-ATPG / Post-ATPG
(Gated Clock Disabling)



Test Vector Manipulation

In-ATPG
(Constraint-Based ATPG)
Post-ATPG
(Low-Capture-Power X-Filling)

Capture Power Reduction: An Example

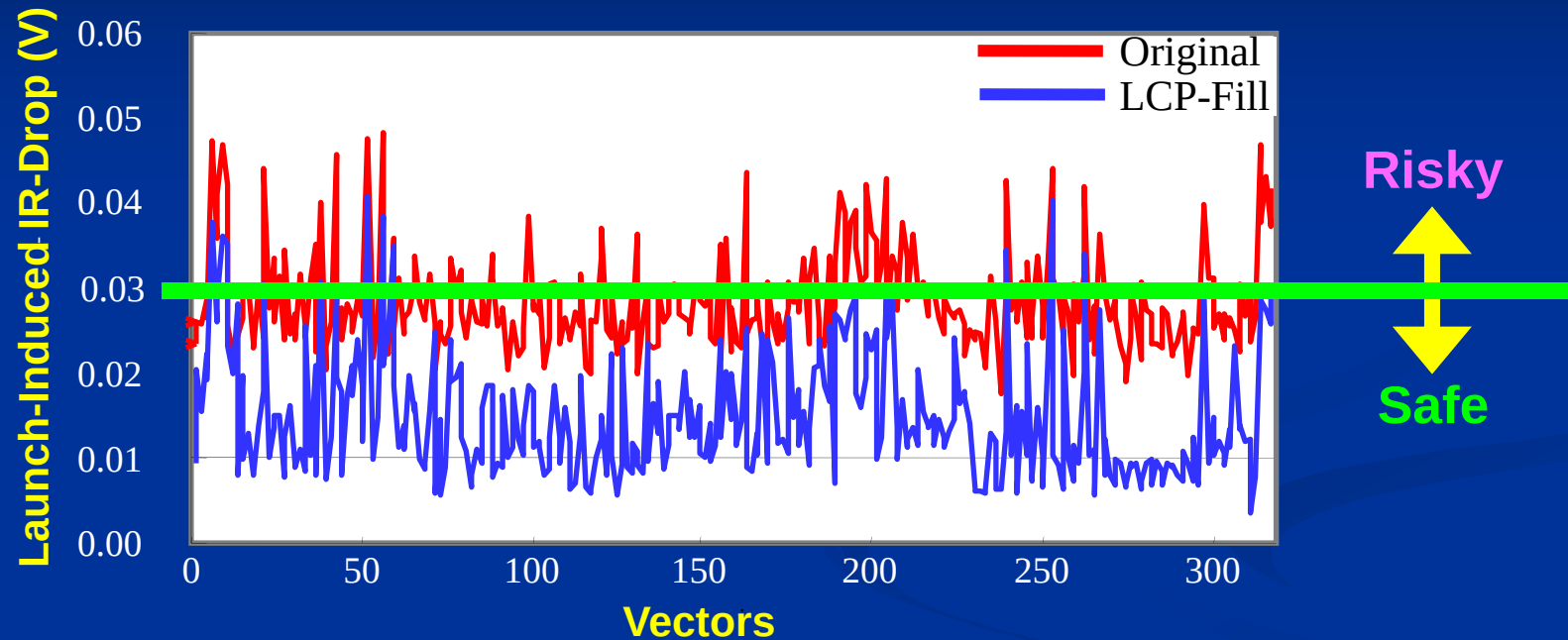


Easy to implement. No or little test data increase.

Capture Power Reduction: *Evaluation Results*

Industrial Circuit

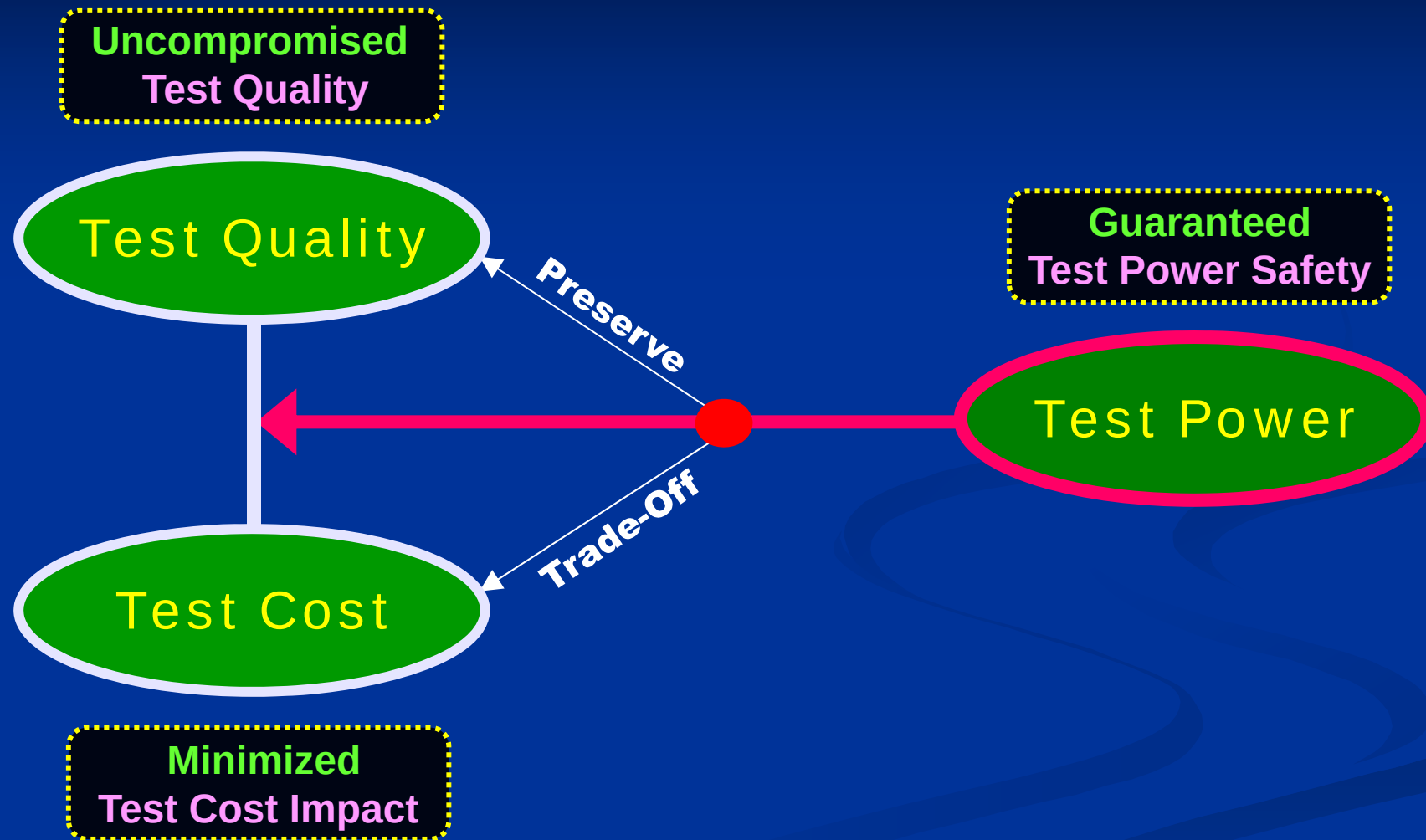
(90nm process / 1.2V / 50K gates / 2.5% VDD IR-drop budget)



Outline

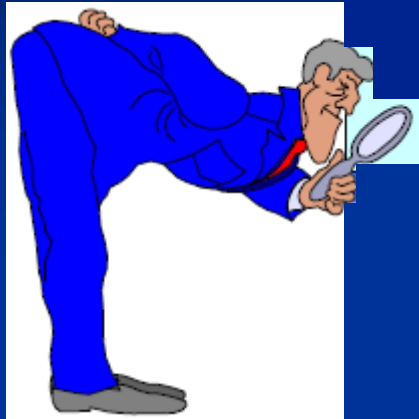
- ① Power: Excitement for Design Engineers
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Ultimate Goals of Power-Aware Testing



Current Problems

Problem: *Lack of Information on Test Power Impact*



- *Which test vector is power-risky ?*
- *What type of power (average shift, peak shift, capture) causing the problem ?*
- *Which part of the chip suffers from excessive test power ?*



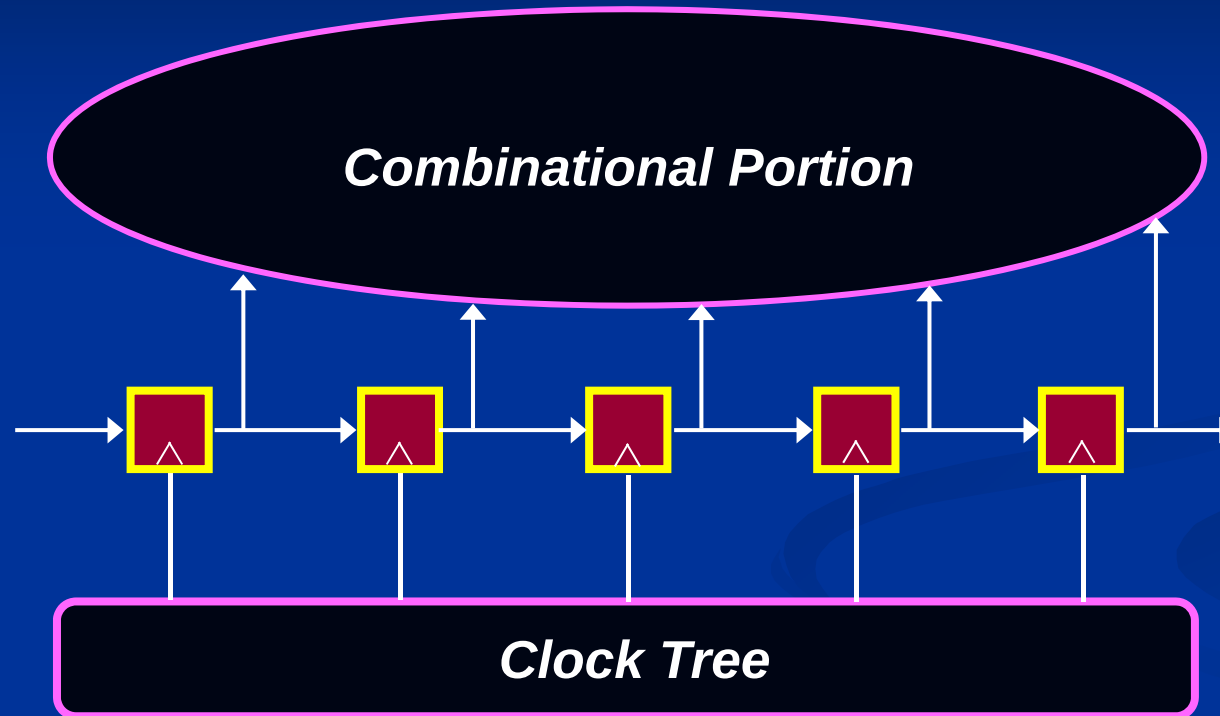
Fast and Accurate Test Power Analysis Needed

Problem: Severe Clock Skew during Scan Shift



Excessive Heat

← *Good Solutions*

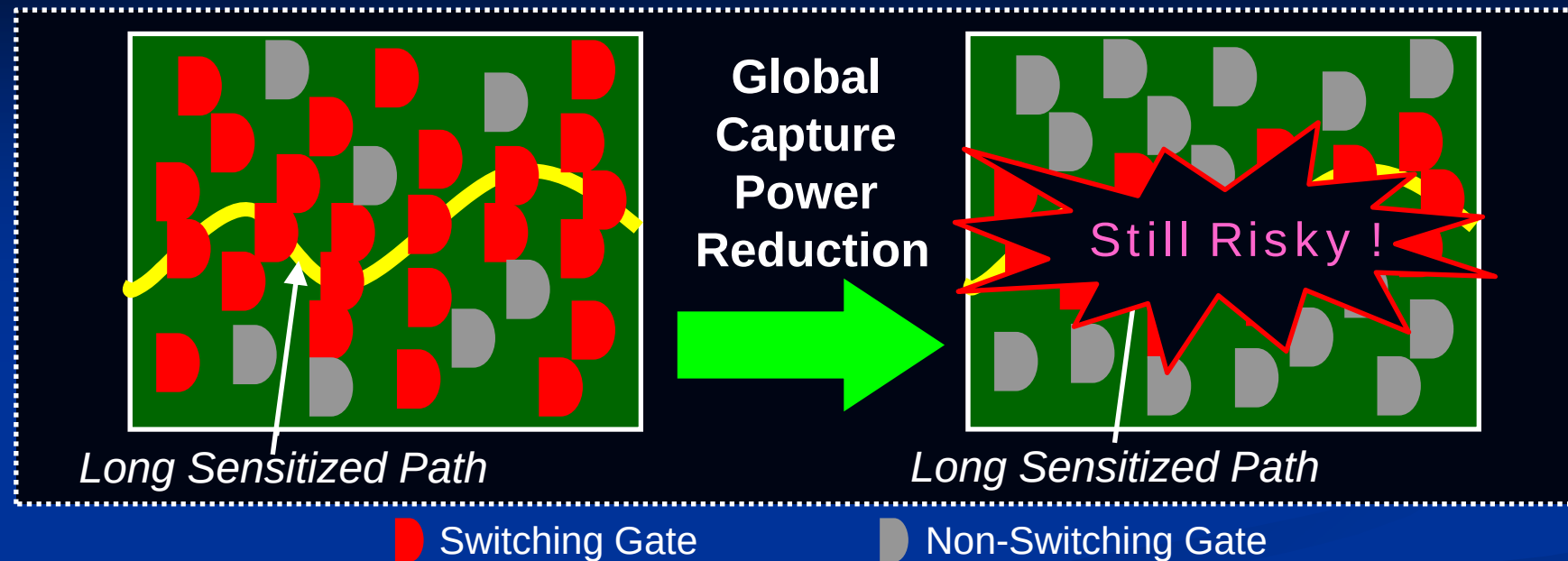


Excessive Clock Skew



Local Peak Scan Shift Power Management Needed

Problem: *Low-Capture-Power* $\neq$ *Capture-Power-Safe*

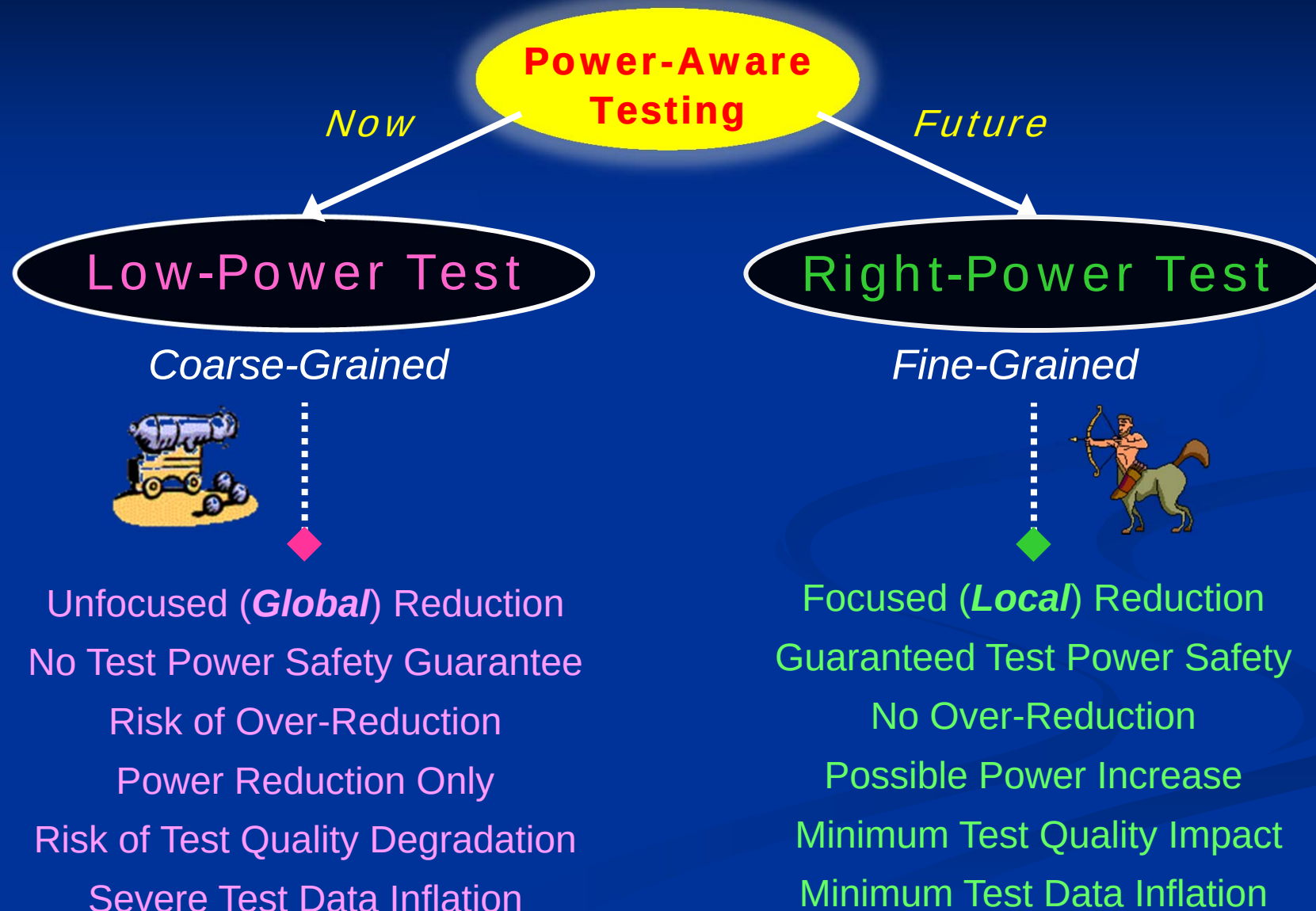


Circuit	# of Gates	# of FFs	# of Clock Gators	# of Test Vectors	Test Power Analysis				
					# of Risky Test Vec.	Ave. Sens. Paths / Vec.	Ave. Risky. Paths / Vec.	CPU (sec.)	# of Risky Vec. with Low WSA
Small	50K	1,077	66	319	8	0.1	1.1	48	3
Large	600K	35,566	984	191	11	0.2	3.8	2,772	5

Local Capture Power Management Needed

Next Stage

Paradigm Shift



Some Interesting Topics (in random order)

- Power-Aware 3D Testing
- Power-Aware FPGA Testing
- Power-Aware On-Line Testing
- Low-Overhead Power-Safe BIST
- Right-Shift-Power Test Generation
- Power-Aware Fault Tolerance Design
- Right-Capture-Power Test Generation
- Fast and Accurate Power Safety Checking
- System-Level Power-Aware Test Scheduling
- Low-Overhead Power-Safe Scan Test Compression
- Fault Diagnosis and Silicon Debug of Low-Power Circuits
- IP with Power-Aware Test Infrastructure and Right-Power Test Data
- Seamless Power-Aware DFT based on CPF or UPF (IEEE Std. 1801-2009)

In Other Words

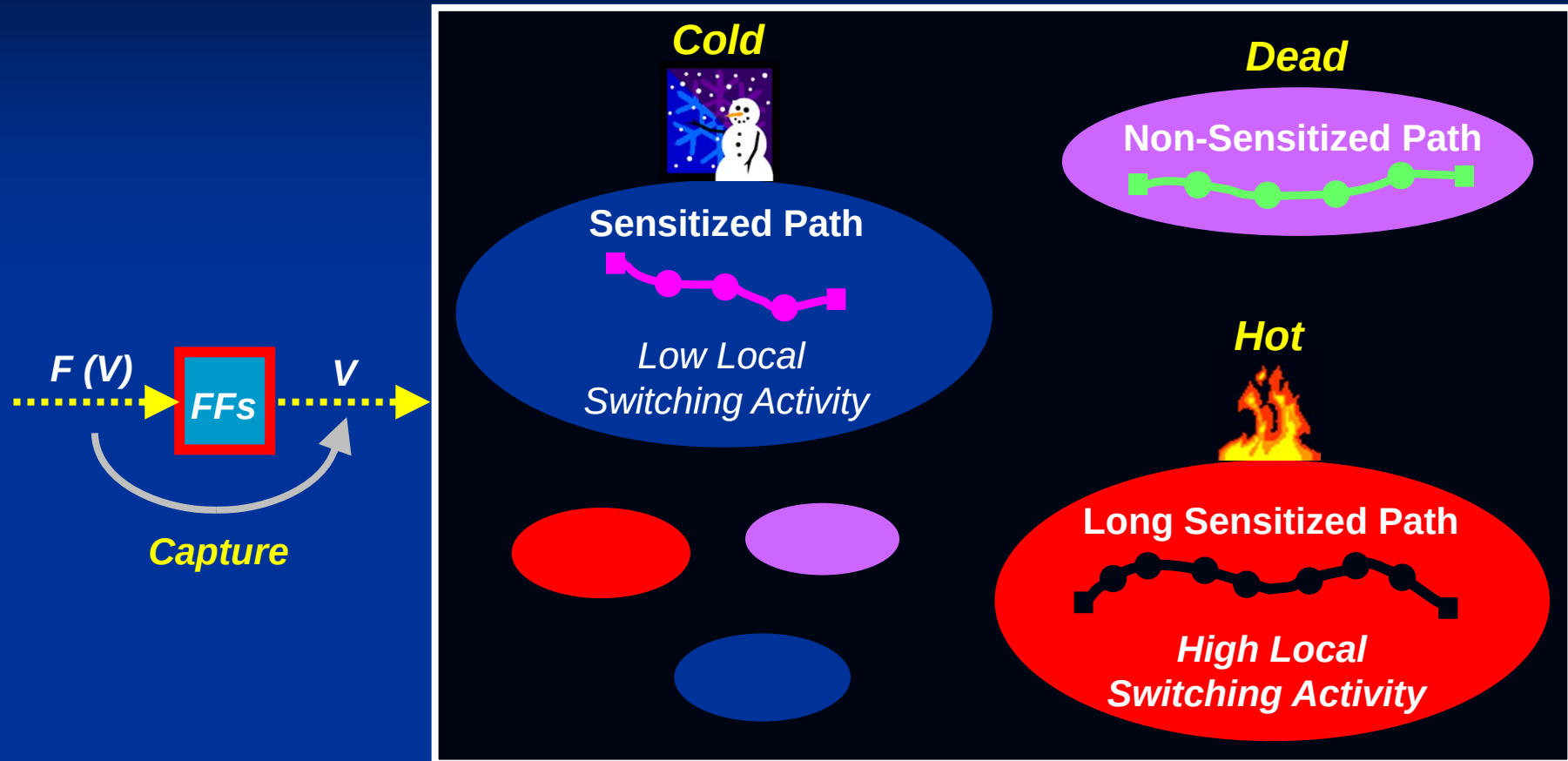
**There are still plenty of new opportunities
in power-aware testing
for research and business.**



Some Interesting Topics (in random order)

- Power-Aware 3D Testing
- Power-Aware FPGA Testing
- Power-Aware On-Line Testing
- Low-Overhead Power-Safe BIST
- Right-Shift-Power Test Generation
- Power-Aware Fault Tolerance Design
- **Right-Capture-Power Test Generation** ✓
- Fast and Accurate Power Safety Checking
- System-Level Power-Aware Test Scheduling
- Low-Overhead Power-Safe Scan Test Compression
- Fault Diagnosis and Silicon Debug of Low-Power Circuits
- IP with Power-Aware Test Infrastructure and Right-Power Test Data
- Seamless Power-Aware DFT based on CPF or UPF (IEEE Std. 1801-2009)

Right-Capture-Power Test Generation: *Concept*



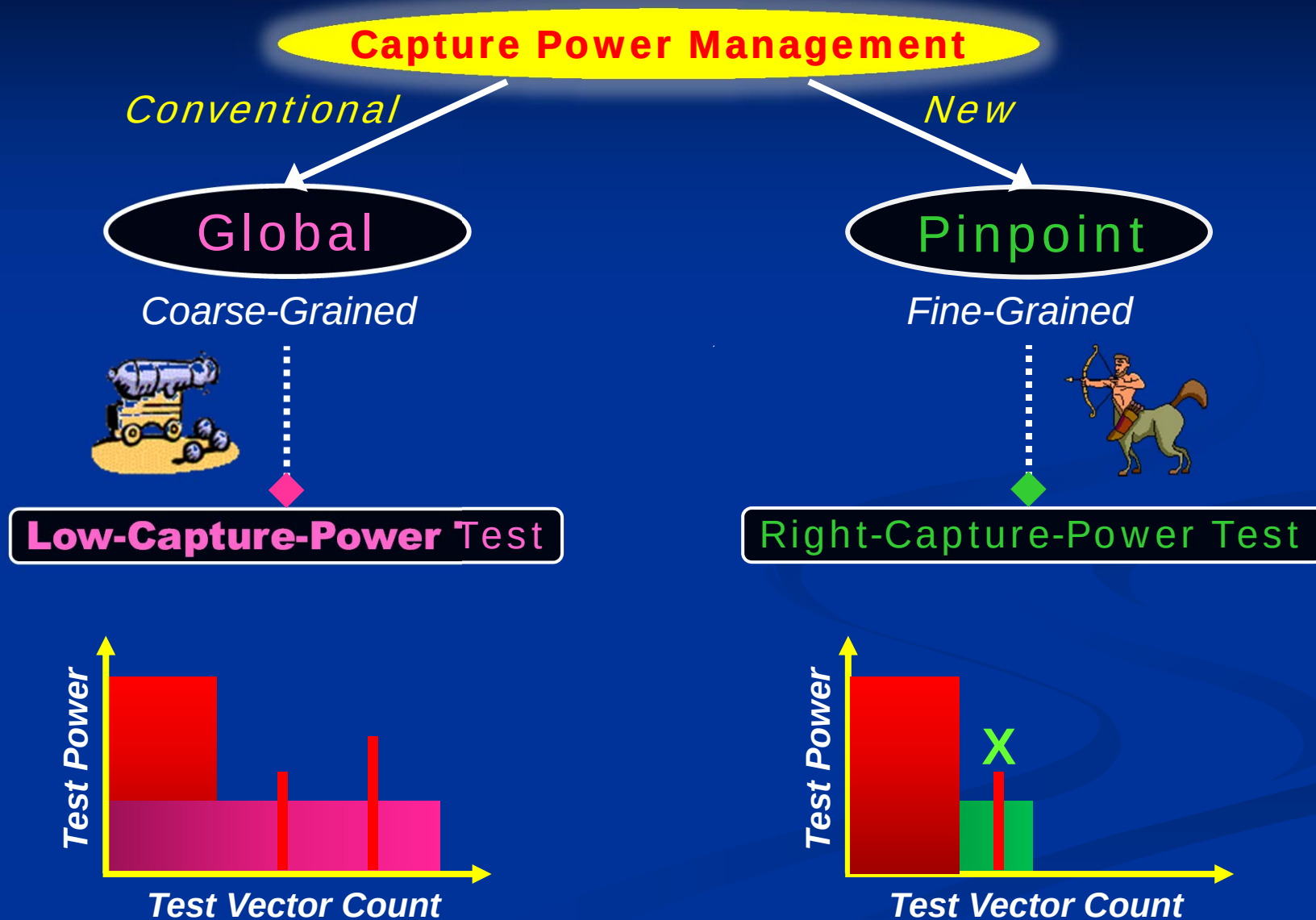
**Pinpoint
Capture
Power
Management**

No need to consider **dead areas**.

Hot areas must be removed by reducing local switching.

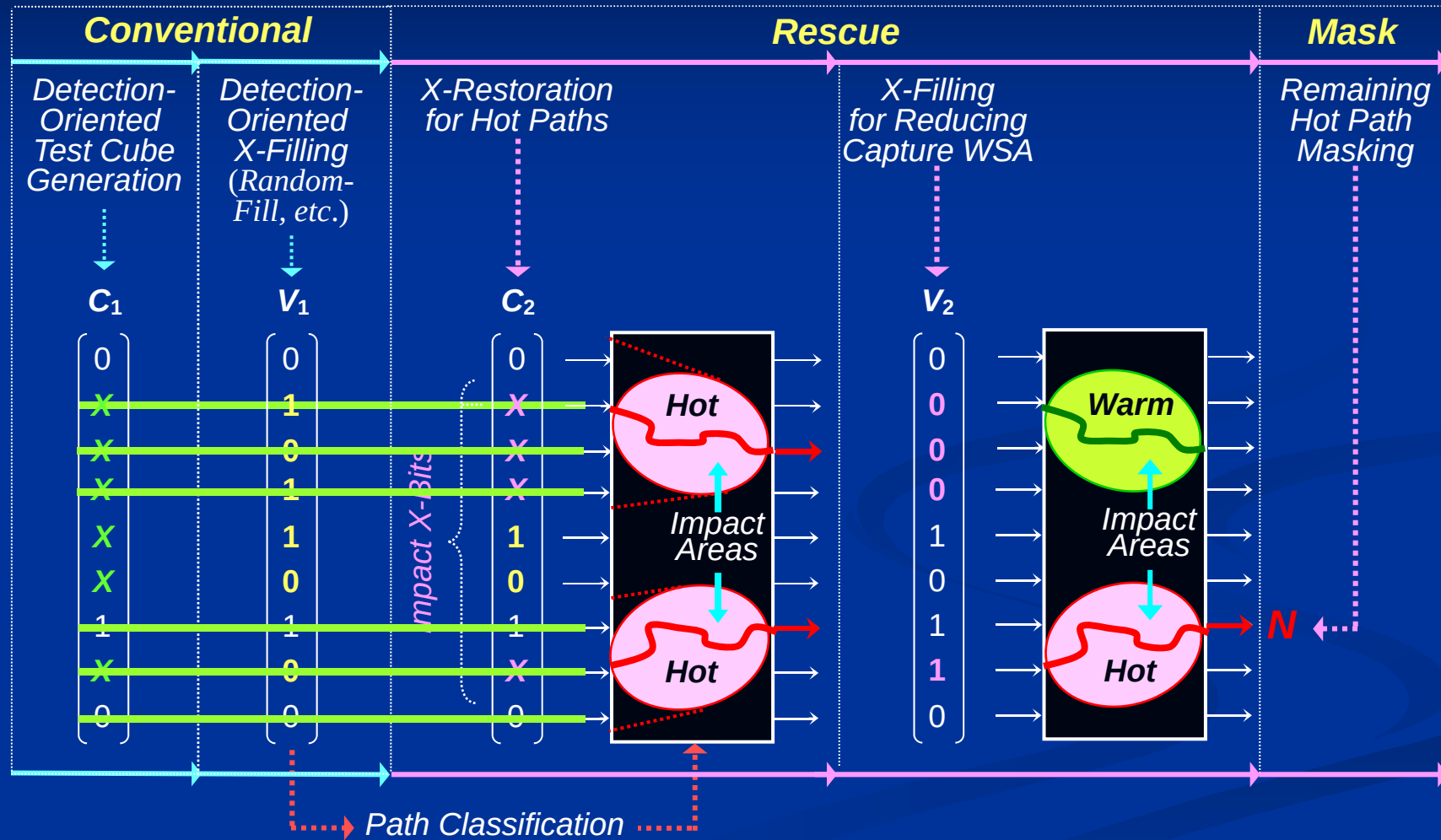
Cold areas may be made "**warm**" by increasing local switching.

Right Capture-Power Test Generation: *Benefits*



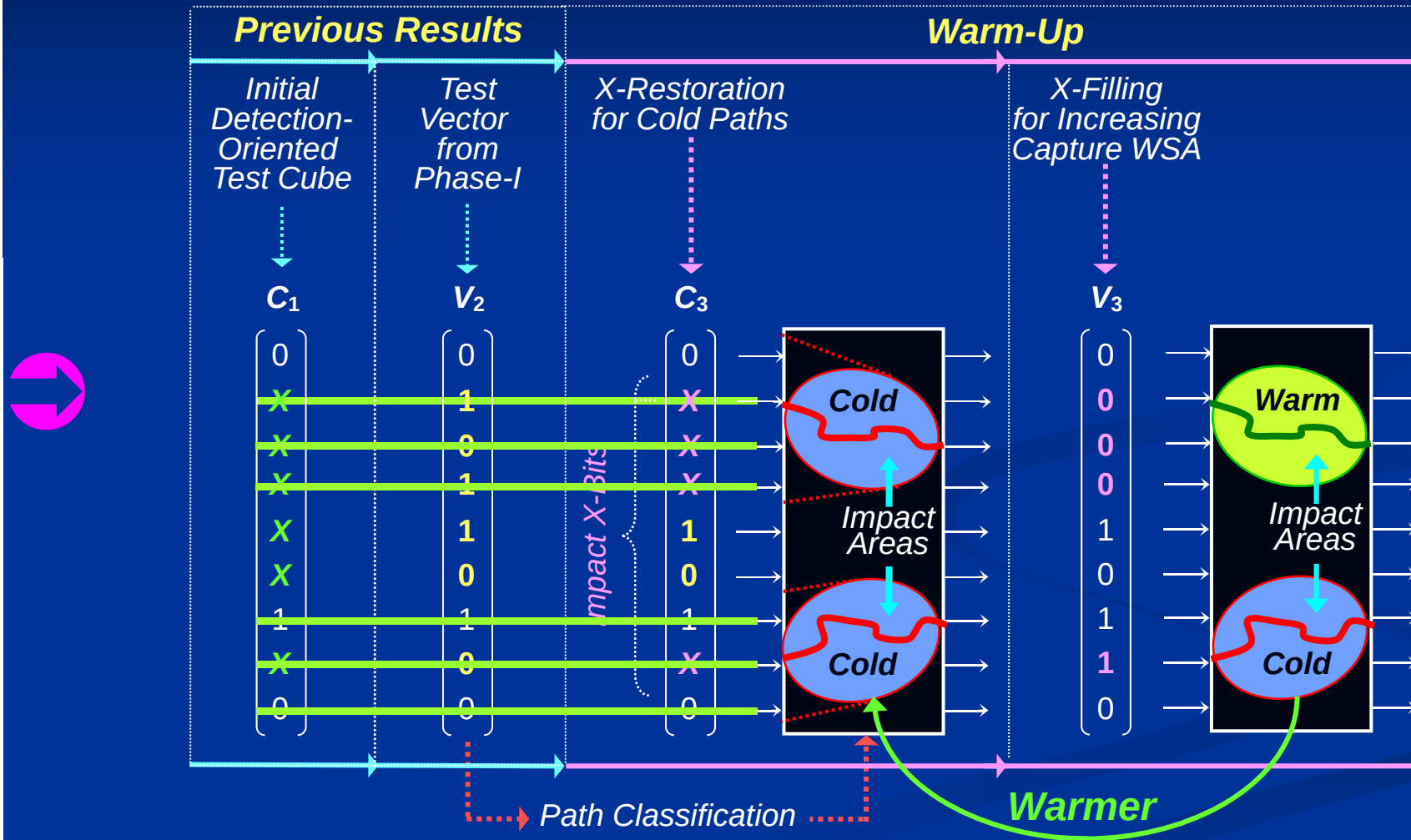
Right Capture-Power Test Generation: *Example*

Phase-I: Hot Path Elimination



Right Capture-Power Test Generation: *Example*

Phase-II: Cold Path Warm-Up



Summary

1

High Performance

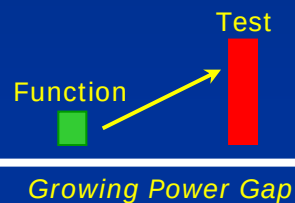
Successful
LSI
Product

Low Power

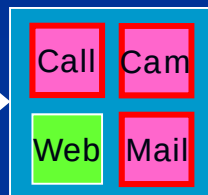
Function-Mode



Low Functional Power
(Wide Use of PMS)

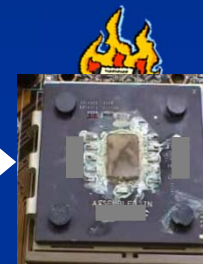


Test-Mode



High Test Power
(Needs to Handle PMS)

Excessive Heat • Timing Failures
Higher Test Complexity due to PMS



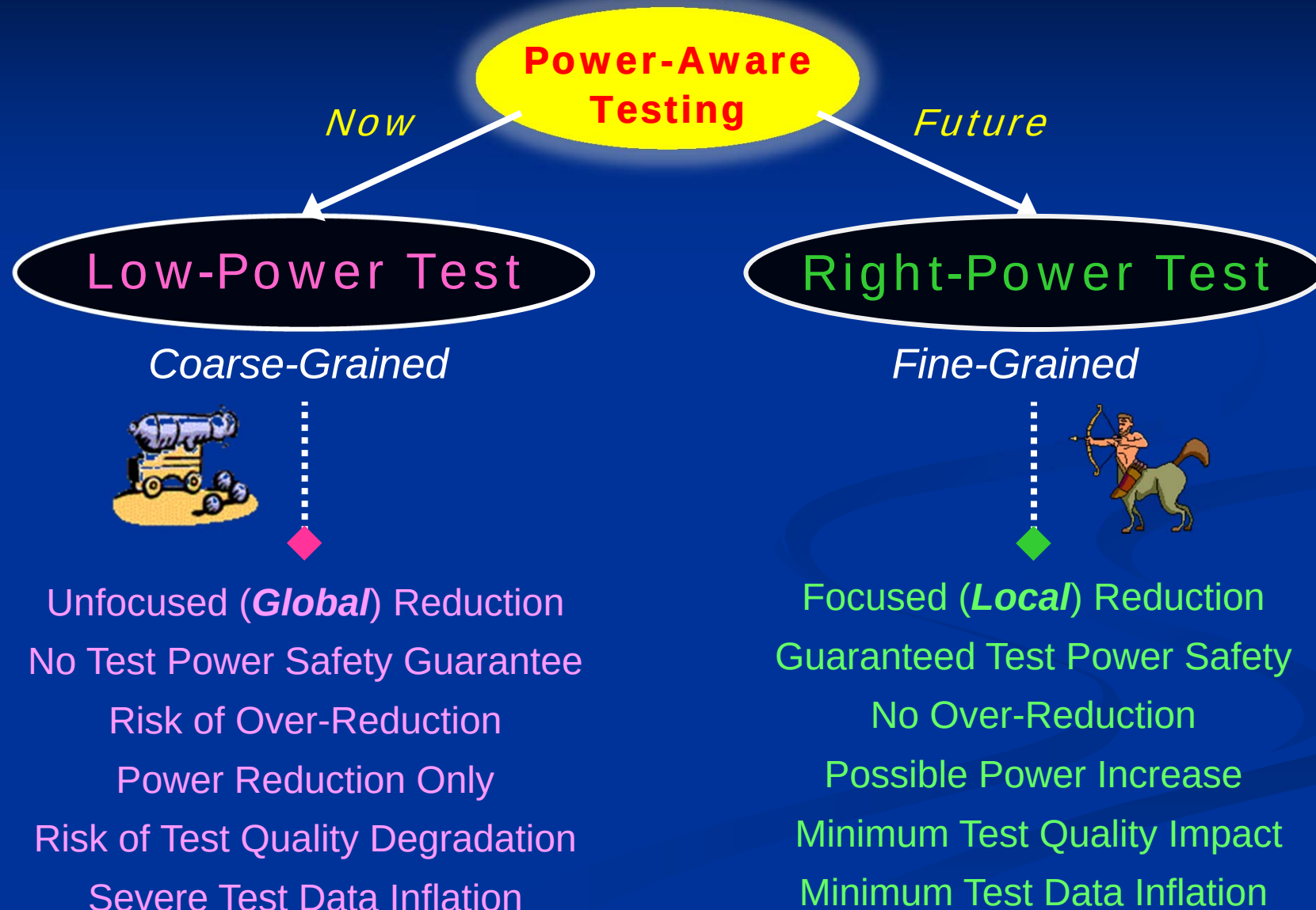
Test Crisis

(Damage / Low Yield / High Cost)

Low
Power
Design

Power
Aware
Test





For More Information

Patrick Girard
Nicola Nicolici
Xiaoqing Wen
EDITORS

Power-Aware Testing and Test Strategies for Low Power Devices

 Springer

For More Activities

Activity Committee on Power-Aware Testing

Test Technology Technical Council (TTTC)
Computer Society
IEEE

Co-Chair: Patrick Girard and Xiaoqing Wen

THANK YOU

*Let us make LSI test **cool**.*

