
The Innovative Analog Applications of FPGA

Poki-Chen

Analog IC LAB, ET, NTUST

Introduction

- Speaker: Associate Prof. Poki Chen
 - Associate Editor, IEEE TVLSI Syst.
 - Director of SoC Research Center, NTUST
- Room: EE807-2 Electronics Engineering Building, NTUST
- Email: poki@mail.ntust.edu.tw
- Website: <http://homepage.ntust.edu.tw/poki/>
- Majors
 - Analog and mixed-mode IC design & layout
 - Time-domain signal processing circuits
 - FPGA-based analog applications



2009 THE-QS Rankings

- Overall: Ranked 351 in the world (QS THES)
- Ranked 72 in Asia 400 / 2009

台灣各大學
2009年泰晤士報世界大學前400名排名

學校名稱	全球排名
台 大	95
清 大	223
成 大	281
陽 明	306
台 科 大	351
交 大	389

製表：記者胡清暉



Analog IC Lab Members

- **Laboratory Aims :**
 - Focused on mixed-mode IC design
 - Excellent paper, patent, IP, and well-trained engineers
- **Laboratory members :**
 - Doctor of Philosophy (PH.D.) : 2
 - Master : 9
 - Bachelor : 7
 - hard-working much required

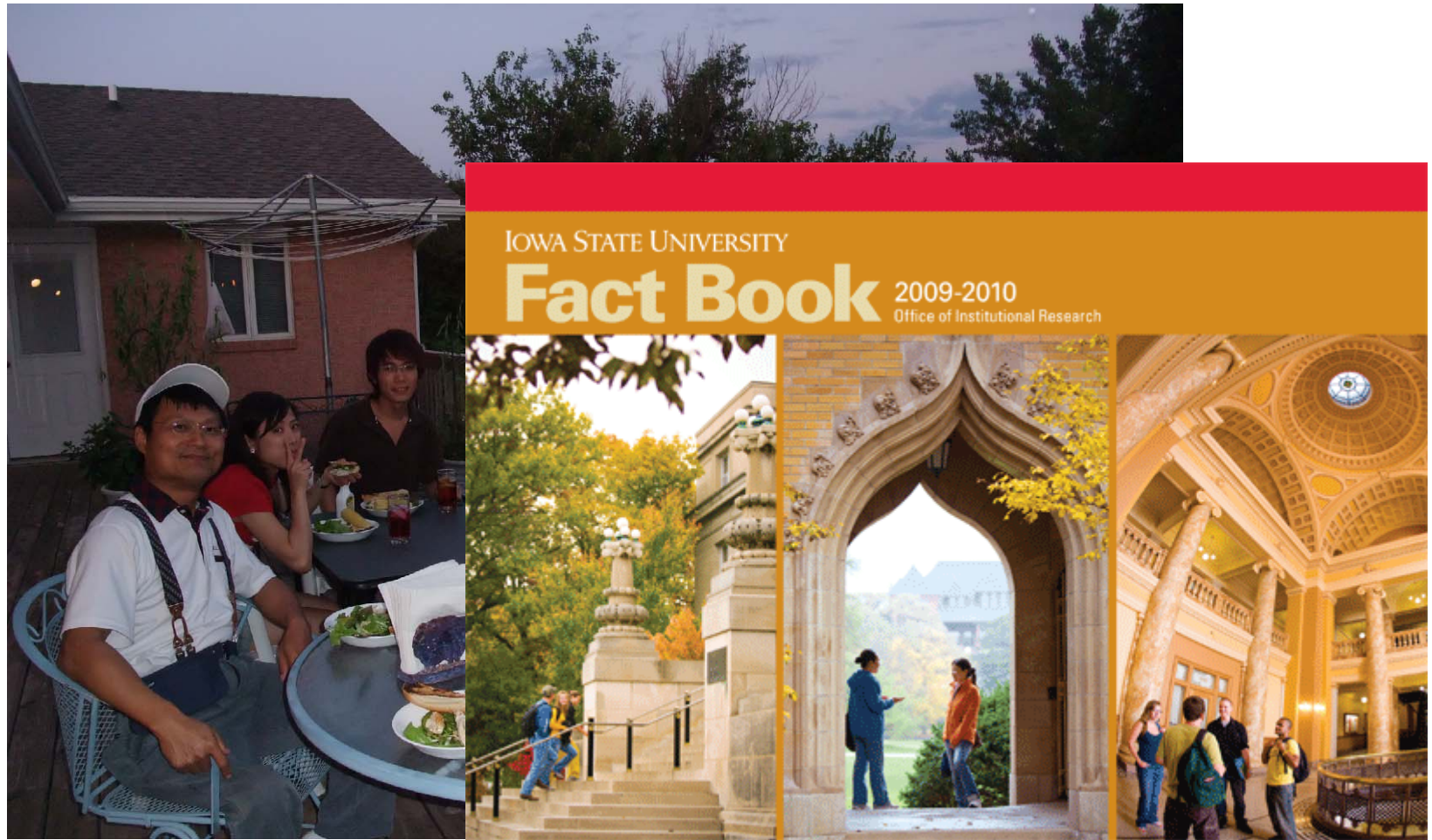
The LAB racing with Time







ISU Visit !



ISU Visit ?



Delft Univ. of Tech. Visit

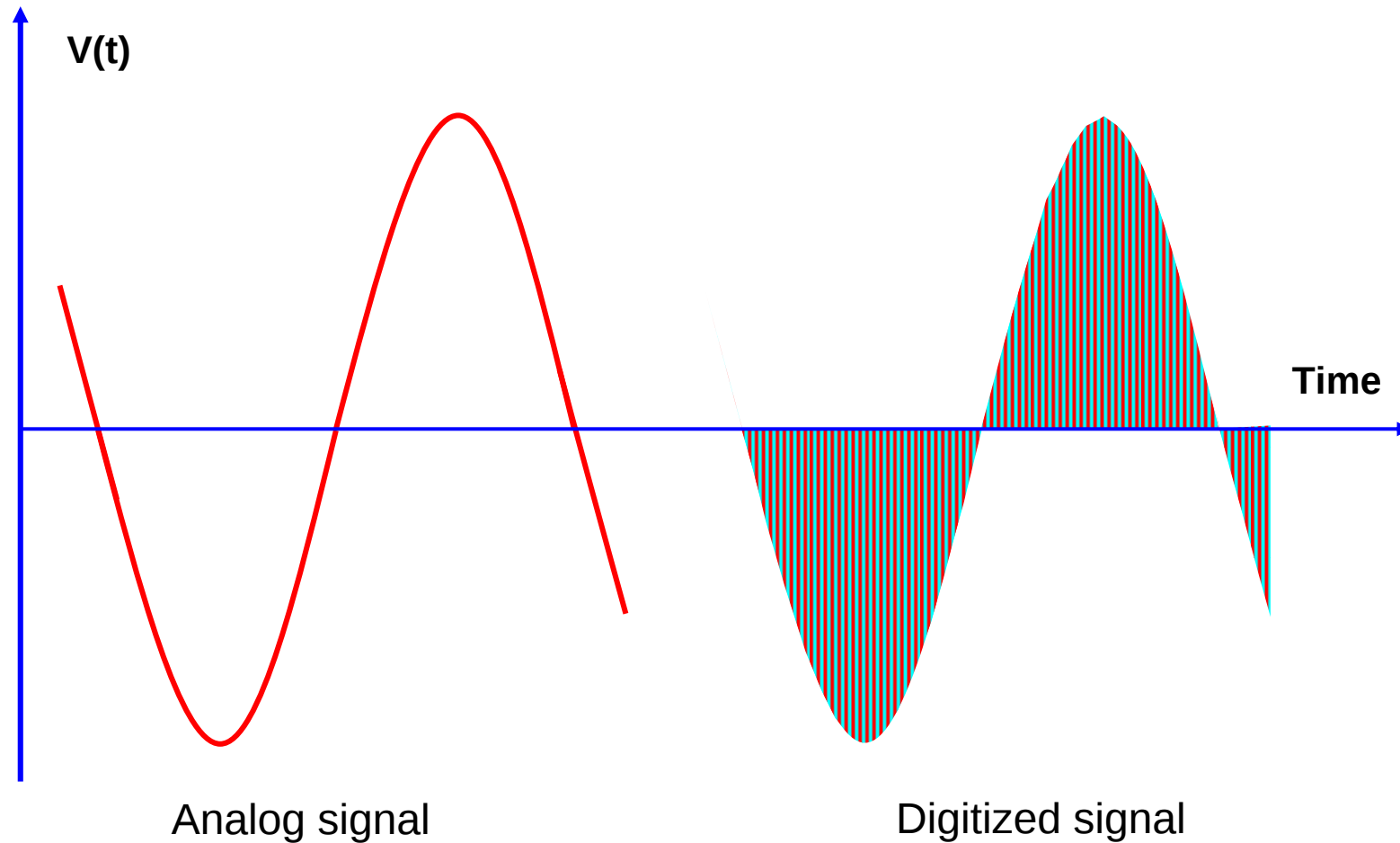


Guidelines

- Motivation
- FPGA Time-to-Digital Converter
- FPGA Digital-to-Time Converter
- FPGA Time-Domain Smart Temperature Sensor
- Future Research Topics

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Analog vs. Digital

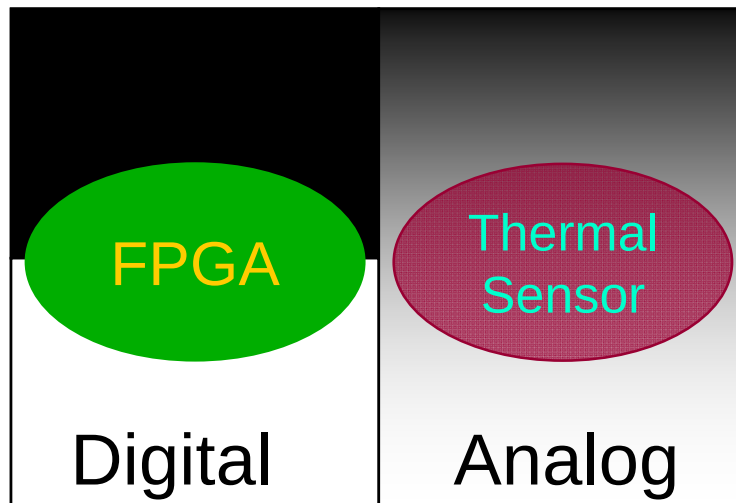


Analogue versus Digital

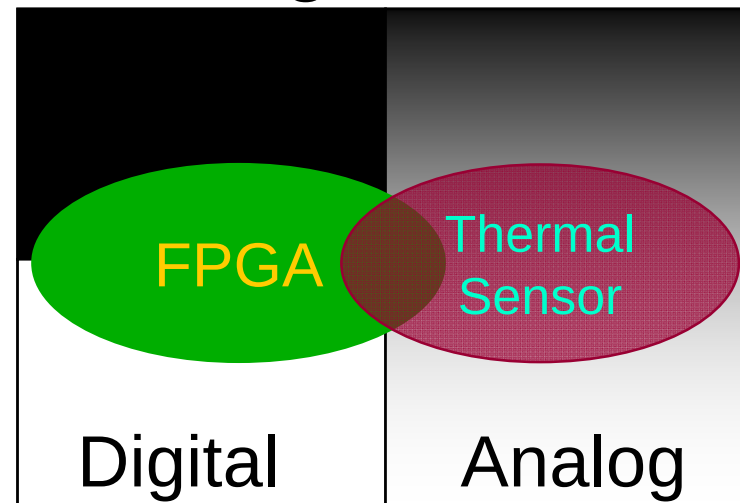
	Analog Design	Digital Design
Signal	Continuous	Discrete
Design	Customized	Standardized
Model requirement	Precise model	Abstract model
Programmability	Hard to change	Programmable by software
Design level	Circuit level	System level
CAD tools	Difficult to use with CAD tools	Amenable to CAD tools
Complexity	Too many design parameters	Simple and easy

Why FPGA

- Fast prototyping
- Easy to port among processes
- Compatible to cell-based design
- More and more built-in analogue blocks



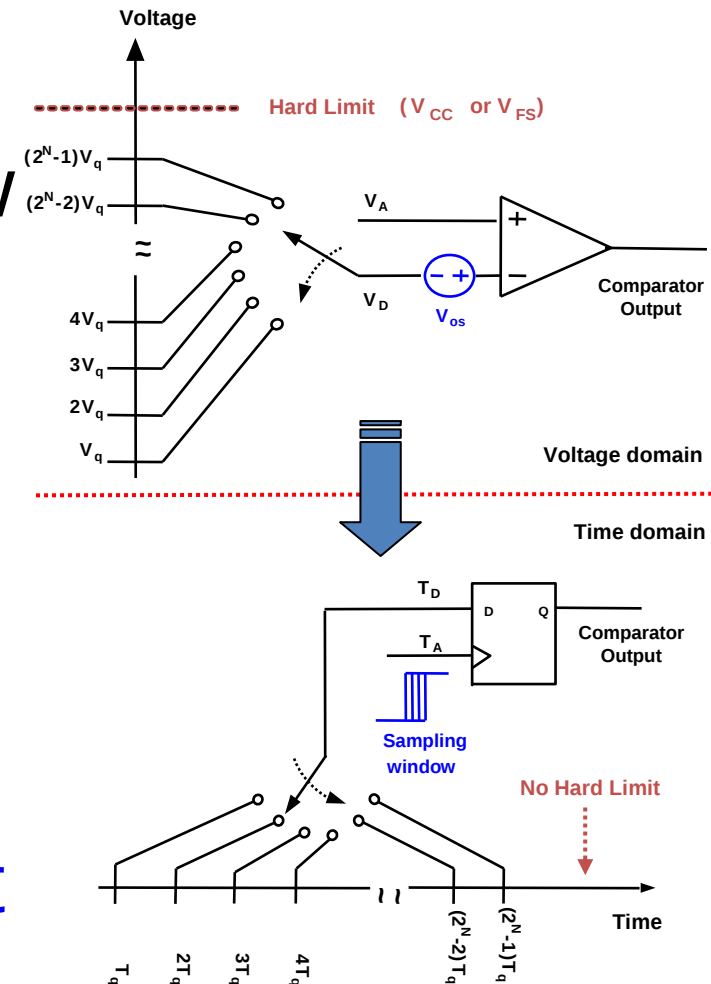
Conventional distribution



Current distribution

Why Time-Domain?

- Supply voltage scalable with process
- Smaller sampling window (dead zone)
- No hard limit for operation range
- Simpler circuit
- Lower chip size and cost
- Possible to digitize circuit

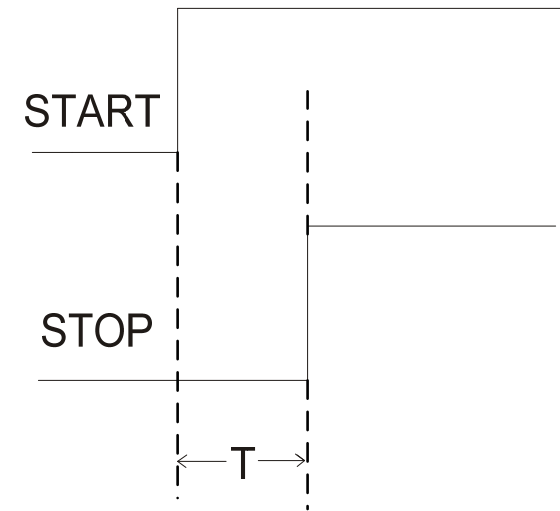
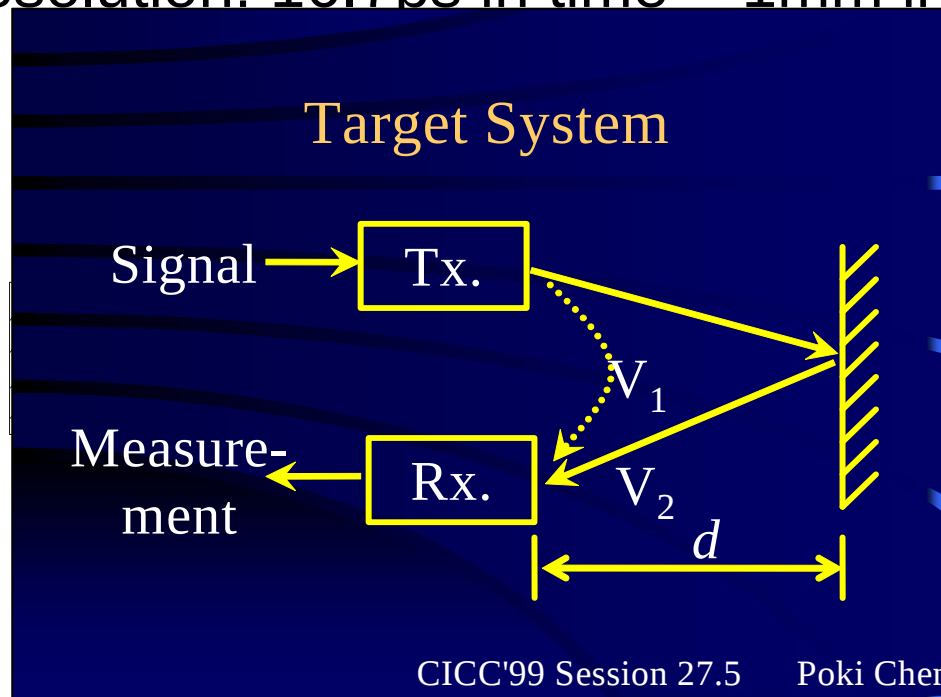


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- Motivation
 - **FPGA Time-to-Digital Converter**
 - FPGA Digital-to-Time Converter
 - FPGA Time-Domain Smart Temperature Sensor
 - Future Research Topics

Applications

- Particle detection for high energy physics
- Phase Demodulation
- Laser ranger
 - Resolution: 16.7ps in time ~ 1mm in distance

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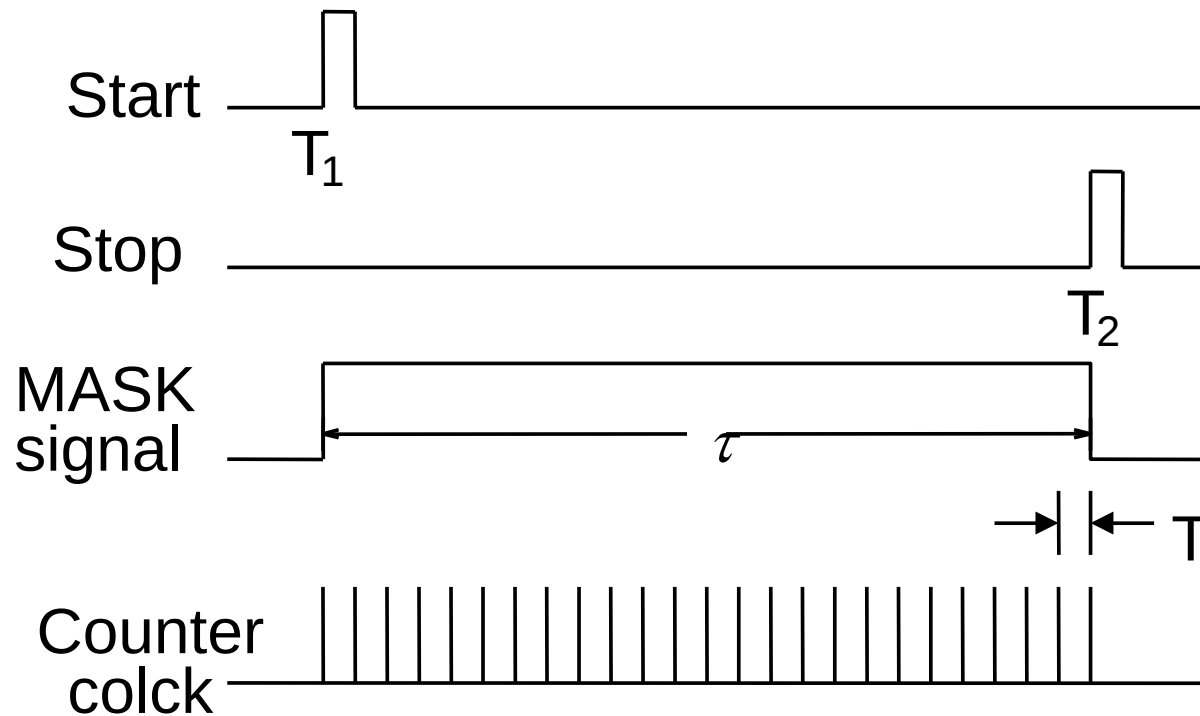


Brief History

- ECL versions
 - Large PCB, high power
- CMOS TDC (1995, JSSC)
 - LSB=780ns, power=15mW
 - single-shot accuracy=3ns
- FPGA TDC (1997, IM)
 - LSB=200ns
 - Trial-and-error realization
- CMOS TDC with cyclic delay line (1997,EL)
 - LSB=286ps
- New pulse-shrinking delay element (1999,CICC)
 - LSB=68ps

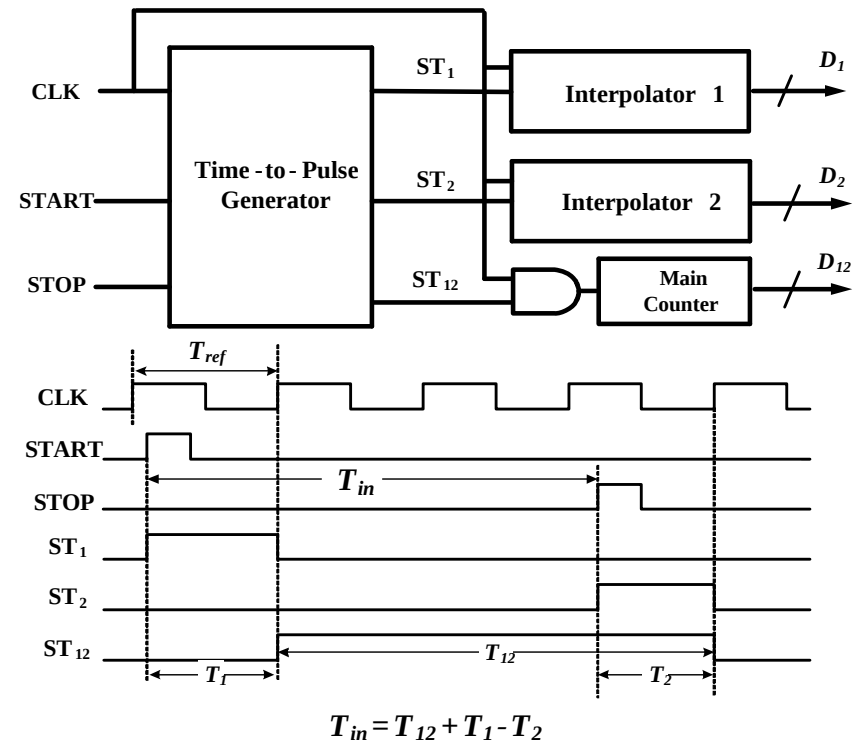
Counter-Based TDC

- Excellent linearity but with poor resolution
- Synchronization problem at both ends



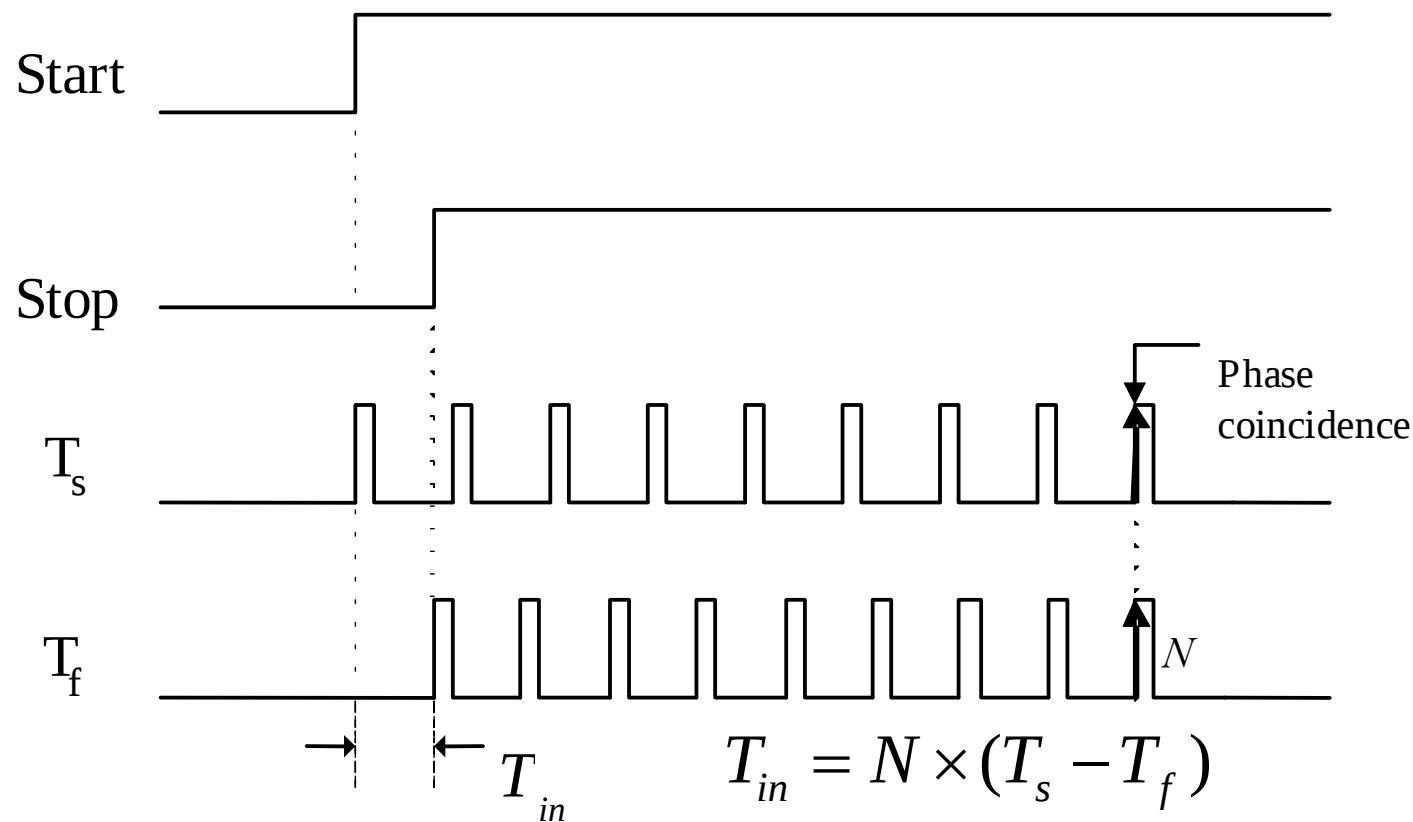
Interpolation Circuit for TDC

- Resolve fractional periods at both ends
- Error caused by mismatch between main & interpolation circuits



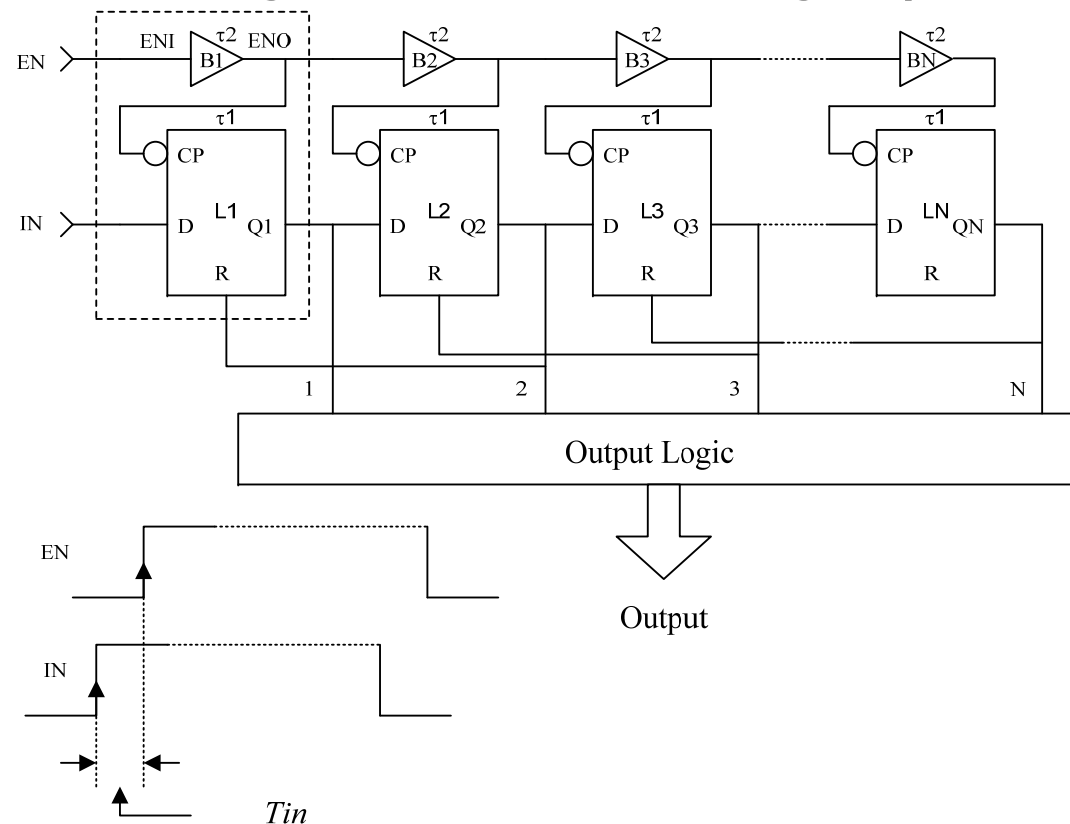
Vernier Principle

- Resolution = period difference

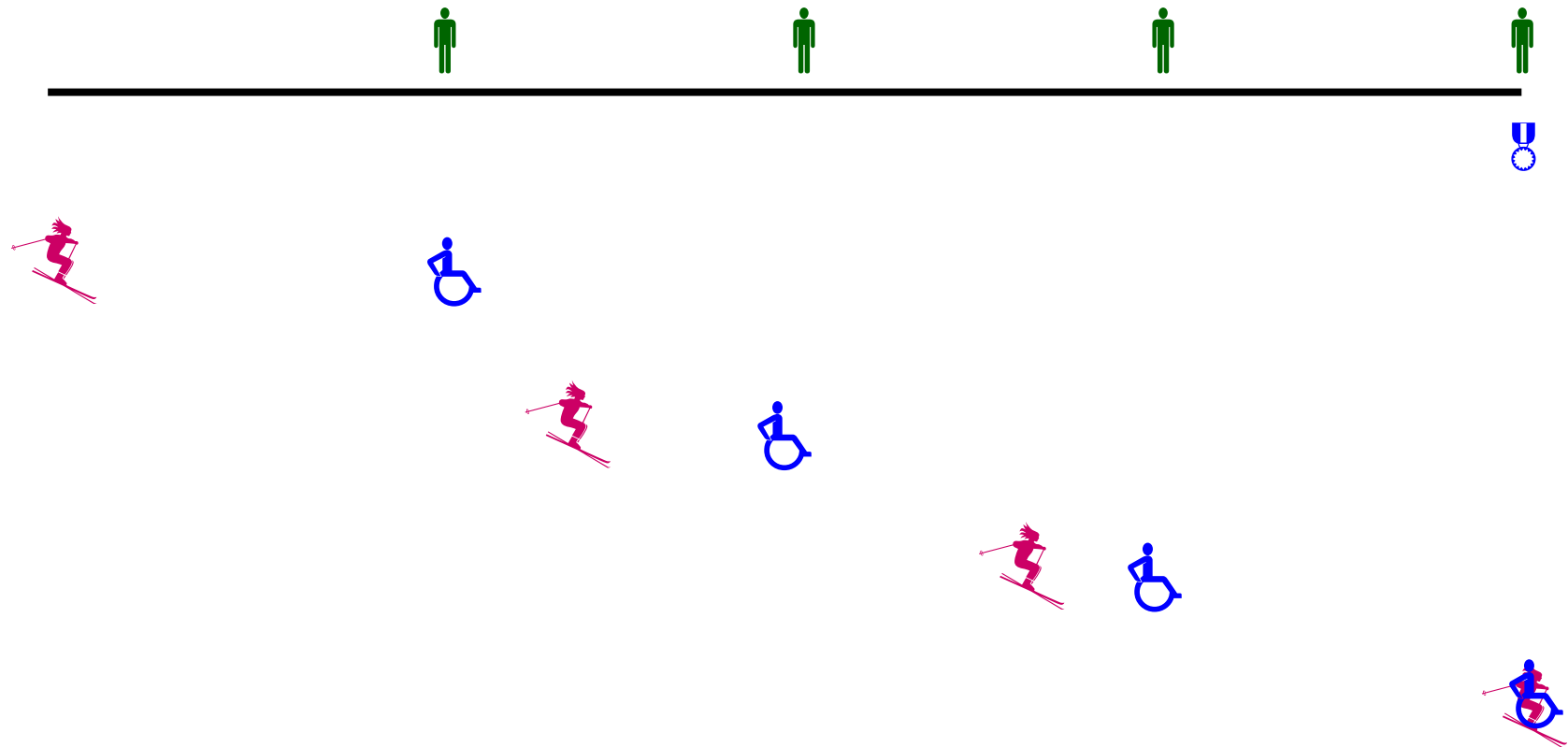


First FPGA TDC

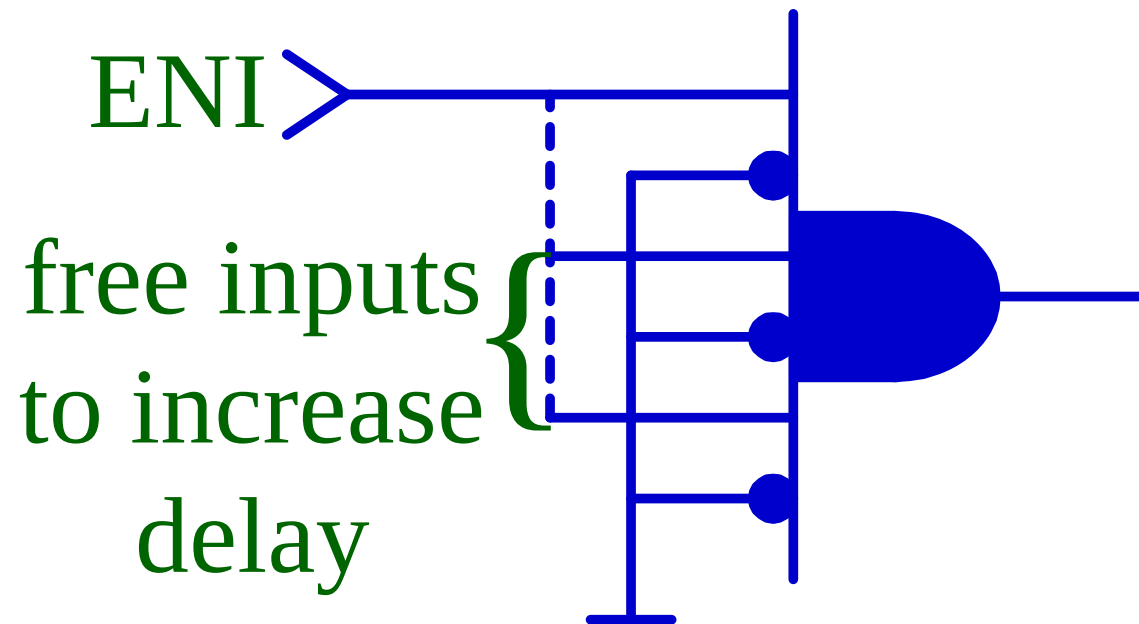
- Based on vernier principle
- Trial-and-error design with QuickLogic pASIC FPGA



Racing in Line



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- Delay controlled by input pins connected



- LSB=200ps
- 20ps resolution achieved in my Lab

J. Kalisz, IM 1997

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 - **FPGA Digital-to-Time Converter**
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Operation Principle: From TDC to DTC

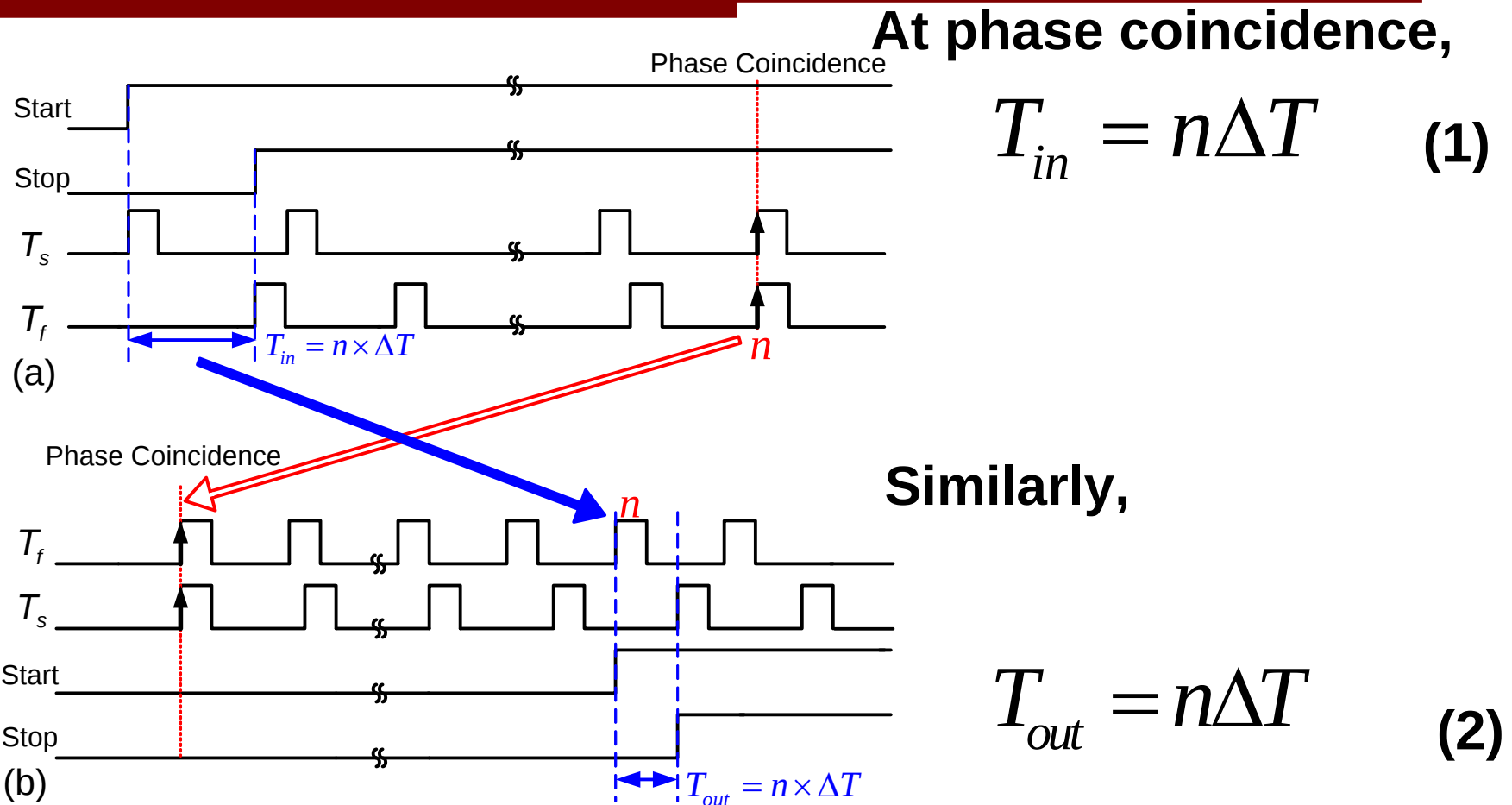
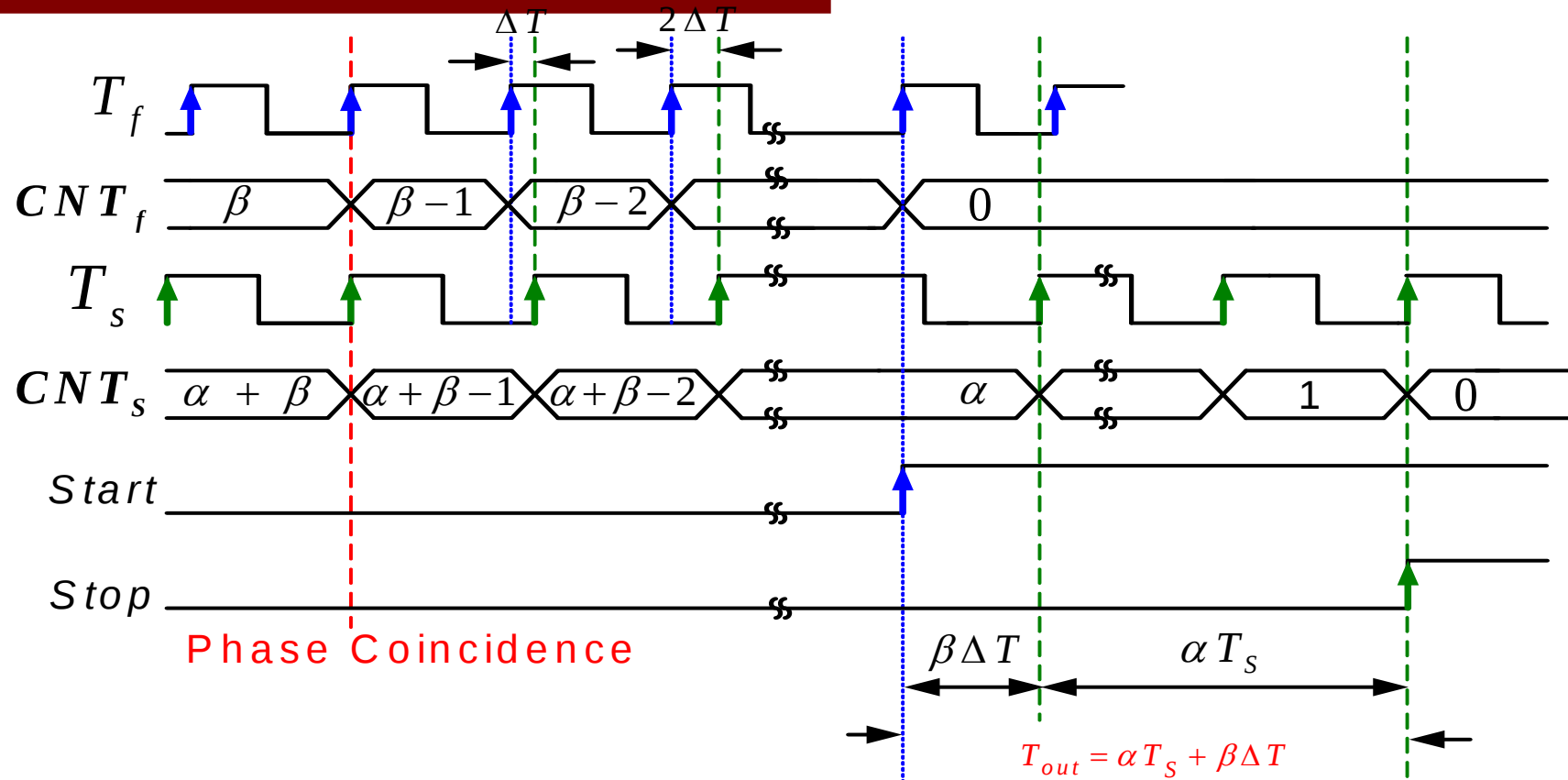


Fig. 1 (a) The vernier TDC, (b) the proposed vernier DTC

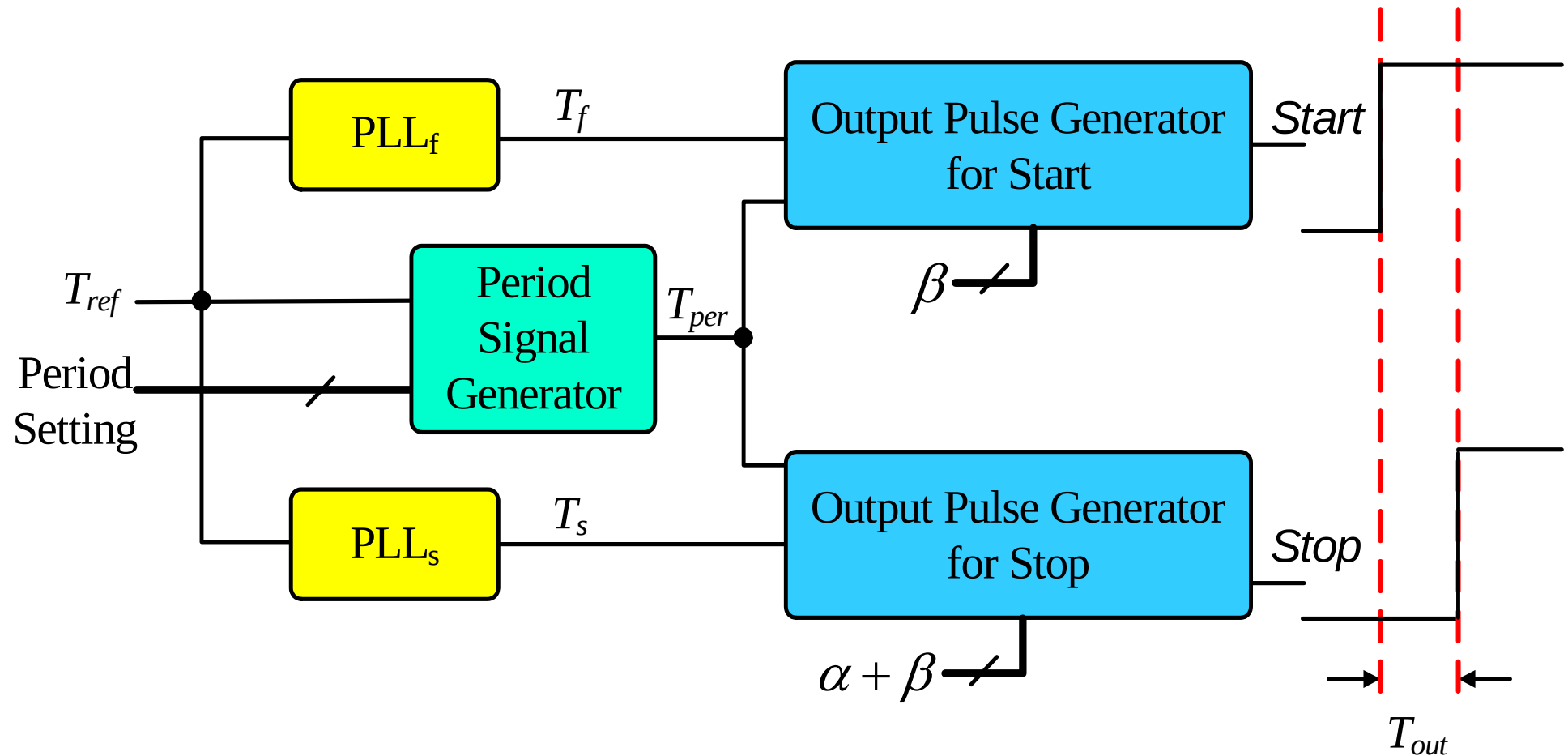
Operation Range Extension with Less Latency



The width of output signal becomes

$$T_{out} = (\alpha + \beta) T_s - \beta T_f = \alpha T_s + \beta (T_s - T_f) = \alpha T_s + \beta \Delta T \quad (4)$$

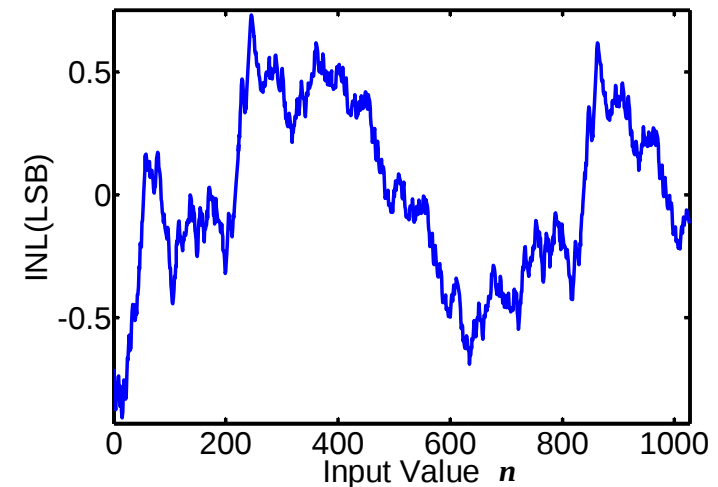
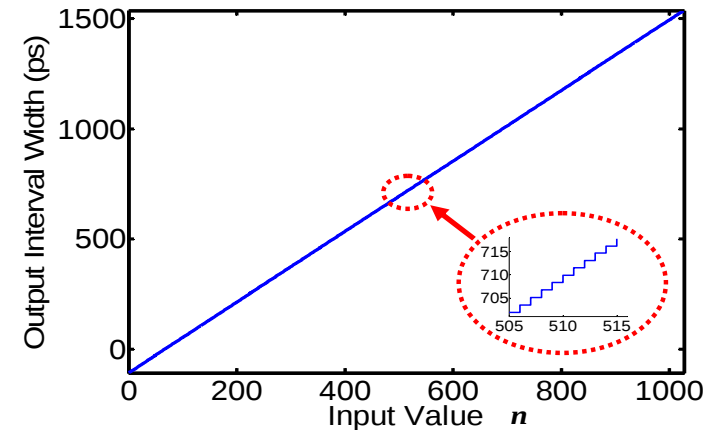
Block Diagram



P. Chen, TCAS-I 2010

FPGA Digital-to-Time Converter

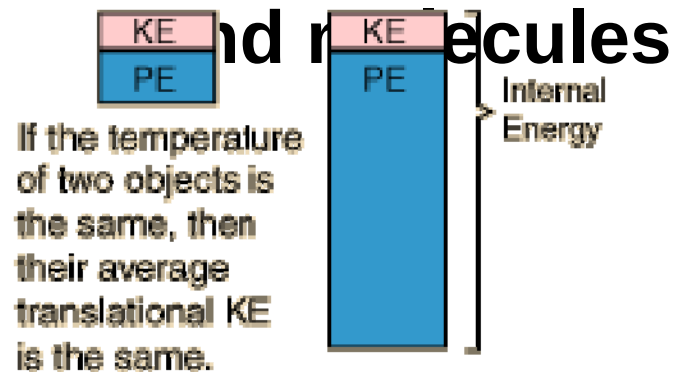
- Xilinx Vertex IV
 - Resolution: 35ps
 - Error: ± 7 ps
- Atera Stratix III
 - Resolution= 1.58ps
 - Error: -0.25~+0.3 ps
- Tsao's paper
 - Resolution: 37.5ps
 - Error~260ps
- Agilent Pulse Generator 81130A
 - Resolution: 2ps
 - Error >100ps
 - List price: US\$ 23k



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What is temperature?

- operational definition
 - a measure of the average translational kinetic energy associated with the disordered microscopic motion of atoms

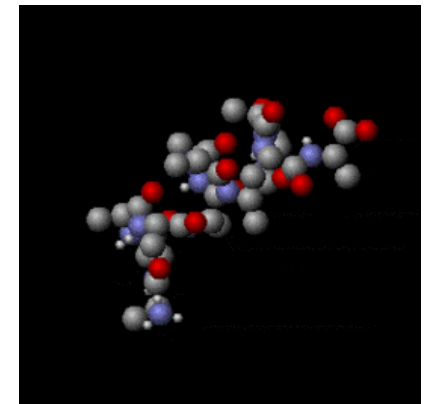
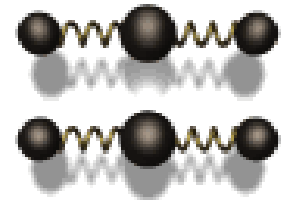


Their internal energies and specific heats will not necessarily be the same.

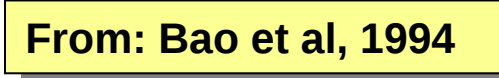
$$\left[\frac{1}{2}mv^2 \right]_{\text{average}} = \frac{3}{2}kT$$

defines the kinetic temperature

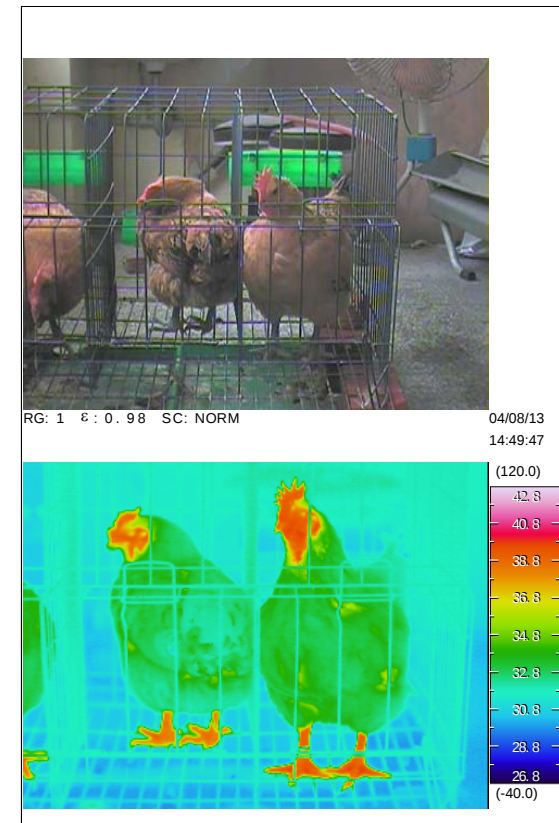
k = Boltzmann constant



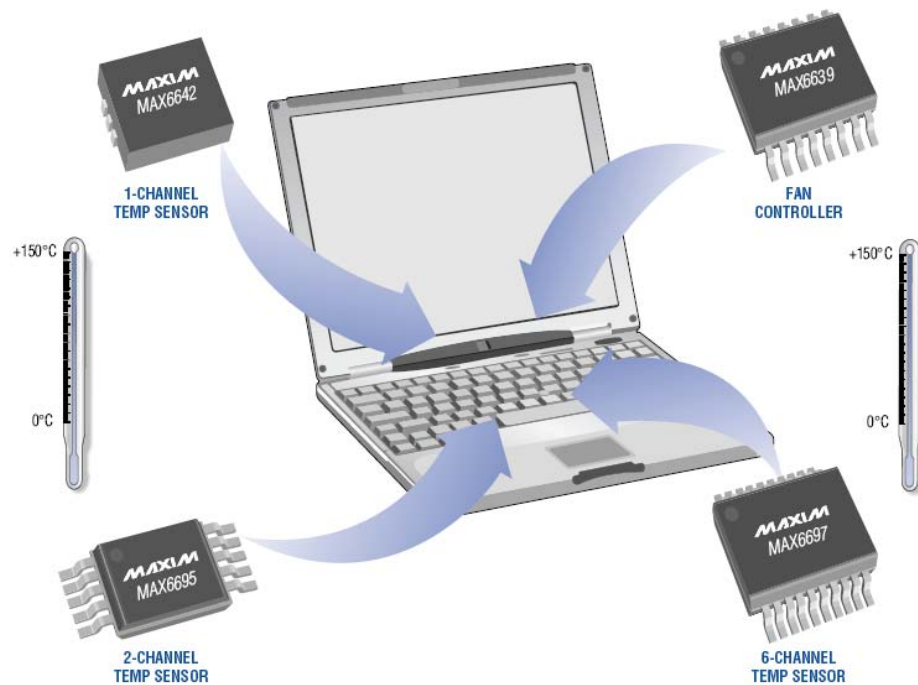
1.1 Introduction 1.2 Background 1.3 Objectives 1.4 Scope 1.5 Methodology 1.6 Results 1.7 Conclusion 1.8 References 1.9 Appendix 1.10 Index 1.11 Glossary 1.12 Abbreviations 1.13 Acronyms 1.14 Footnotes 1.15 Endnotes 1.16 References 1.17 Appendix 1.18 Index 1.19 Glossary 1.20 Abbreviations 1.21 Acronyms 1.22 Footnotes 1.23 Endnotes 1.24 References 1.25 Appendix 1.26 Index 1.27 Glossary 1.28 Abbreviations 1.29 Acronyms 1.30 Footnotes 1.31 Endnotes 1.32 References 1.33 Appendix 1.34 Index 1.35 Glossary 1.36 Abbreviations 1.37 Acronyms 1.38 Footnotes 1.39 Endnotes 1.40 References 1.41 Appendix 1.42 Index 1.43 Glossary 1.44 Abbreviations 1.45 Acronyms 1.46 Footnotes 1.47 Endnotes 1.48 References 1.49 Appendix 1.50 Index 1.51 Glossary 1.52 Abbreviations 1.53 Acronyms 1.54 Footnotes 1.55 Endnotes 1.56 References 1.57 Appendix 1.58 Index 1.59 Glossary 1.60 Abbreviations 1.61 Acronyms 1.62 Footnotes 1.63 Endnotes 1.64 References 1.65 Appendix 1.66 Index 1.67 Glossary 1.68 Abbreviations 1.69 Acronyms 1.70 Footnotes 1.71 Endnotes 1.72 References 1.73 Appendix 1.74 Index 1.75 Glossary 1.76 Abbreviations 1.77 Acronyms 1.78 Footnotes 1.79 Endnotes 1.80 References 1.81 Appendix 1.82 Index 1.83 Glossary 1.84 Abbreviations 1.85 Acronyms 1.86 Footnotes 1.87 Endnotes 1.88 References 1.89 Appendix 1.90 Index 1.91 Glossary 1.92 Abbreviations 1.93 Acronyms 1.94 Footnotes 1.95 Endnotes 1.96 References 1.97 Appendix 1.98 Index 1.99 Glossary 1.100 Abbreviations 1.101 Acronyms 1.102 Footnotes 1.103 Endnotes 1.104 References 1.105 Appendix 1.106 Index 1.107 Glossary 1.108 Abbreviations 1.109 Acronyms 1.110 Footnotes 1.111 Endnotes 1.112 References 1.113 Appendix 1.114 Index 1.115 Glossary 1.116 Abbreviations 1.117 Acronyms 1.118 Footnotes 1.119 Endnotes 1.120 References 1.121 Appendix 1.122 Index 1.123 Glossary 1.124 Abbreviations 1.125 Acronyms 1.126 Footnotes 1.127 Endnotes 1.128 References 1.129 Appendix 1.130 Index 1.131 Glossary 1.132 Abbreviations 1.133 Acronyms 1.134 Footnotes 1.135 Endnotes 1.136 References 1.137 Appendix 1.138 Index 1.139 Glossary 1.140 Abbreviations 1.141 Acronyms 1.142 Footnotes 1.143 Endnotes 1.144 References 1.145 Appendix 1.146 Index 1.147 Glossary 1.148 Abbreviations 1.149 Acronyms 1.150 Footnotes 1.151 Endnotes 1.152 References 1.153 Appendix 1.154 Index 1.155 Glossary 1.156 Abbreviations 1.157 Acronyms 1.158 Footnotes 1.159 Endnotes 1.160 References 1.161 Appendix 1.162 Index 1.163 Glossary 1.164 Abbreviations 1.165 Acronyms 1.166 Footnotes 1.167 Endnotes 1.168 References 1.169 Appendix 1.170 Index 1.171 Glossary 1.172 Abbreviations 1.173 Acronyms 1.174 Footnotes 1.175 Endnotes 1.176 References 1.177 Appendix 1.178 Index 1.179 Glossary 1.180 Abbreviations 1.181 Acronyms 1.182 Footnotes 1.183 Endnotes 1.184 References 1.185 Appendix 1.186 Index 1.187 Glossary 1.188 Abbreviations 1.189 Acronyms 1.190 Footnotes 1.191 Endnotes 1.192 References 1.193 Appendix 1.194 Index 1.195 Glossary 1.196 Abbreviations 1.197 Acronyms 1.198 Footnotes 1.199 Endnotes 1.200 References</
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Applications

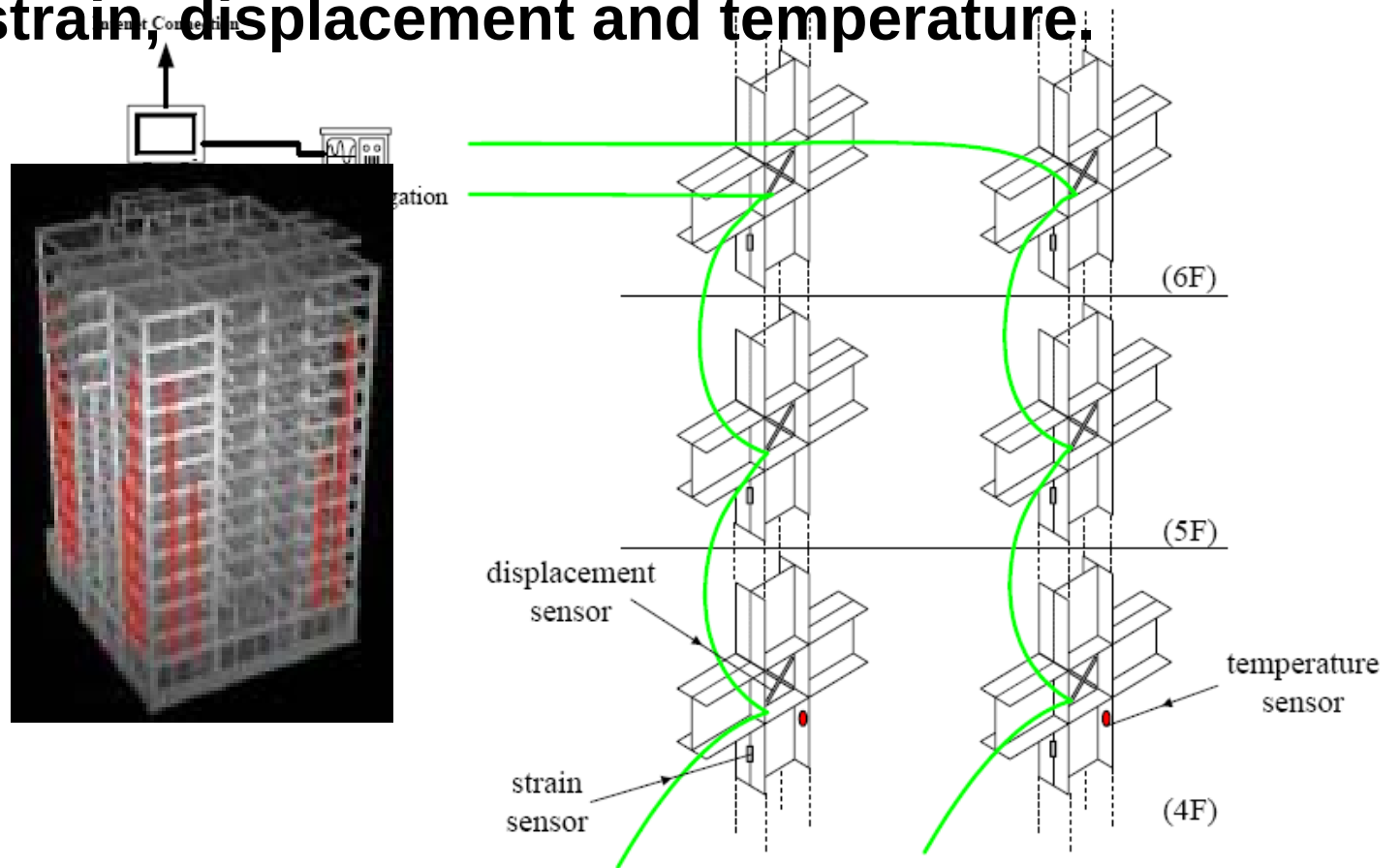


Digital Thermometer

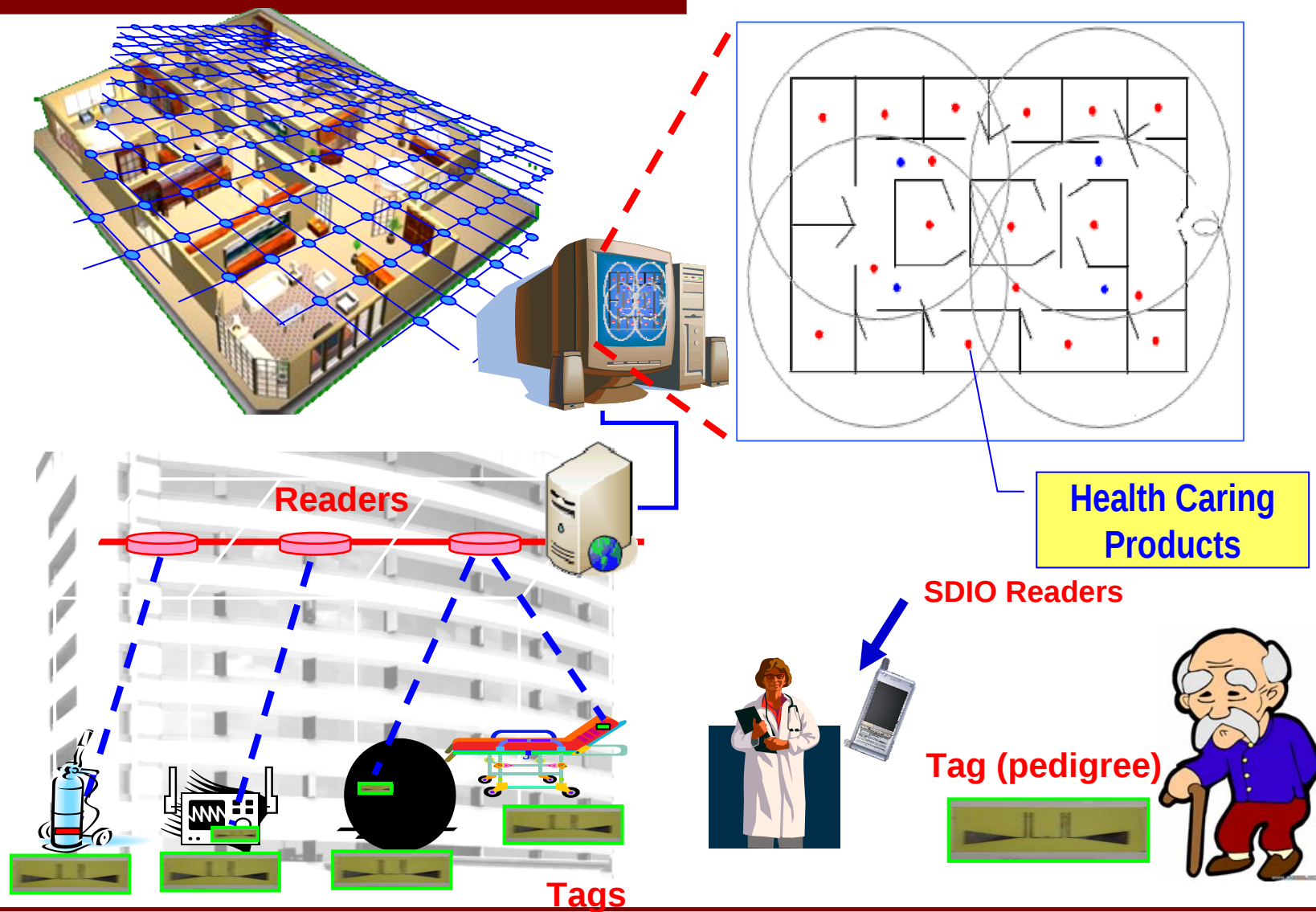


Structural Health Monitoring System

- ensure the structural integrity by monitoring the response of the building.
- measure strain, displacement and temperature.

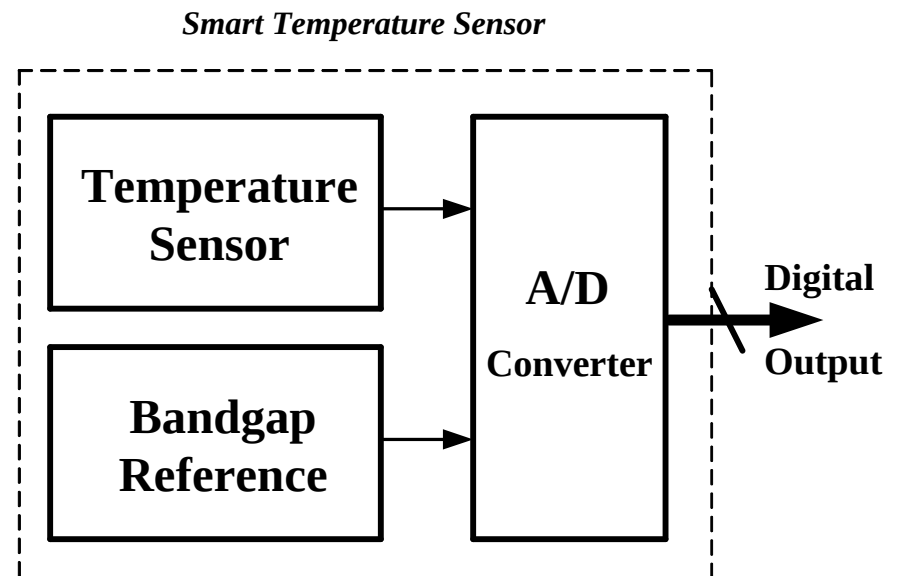


Body Sensor Network



Voltage-Domain Predecessors

- Parasitic BJT used
- Subtle calibration circuits adopted
 - chopping and dynamic element matching (DEM)
 - second-order curvature correction
 - offset cancellation
 - $\Delta \Sigma$ modulator
- High accuracy OPAMP with large number of input bits



Industry's Highest Accuracy Temp Sensors

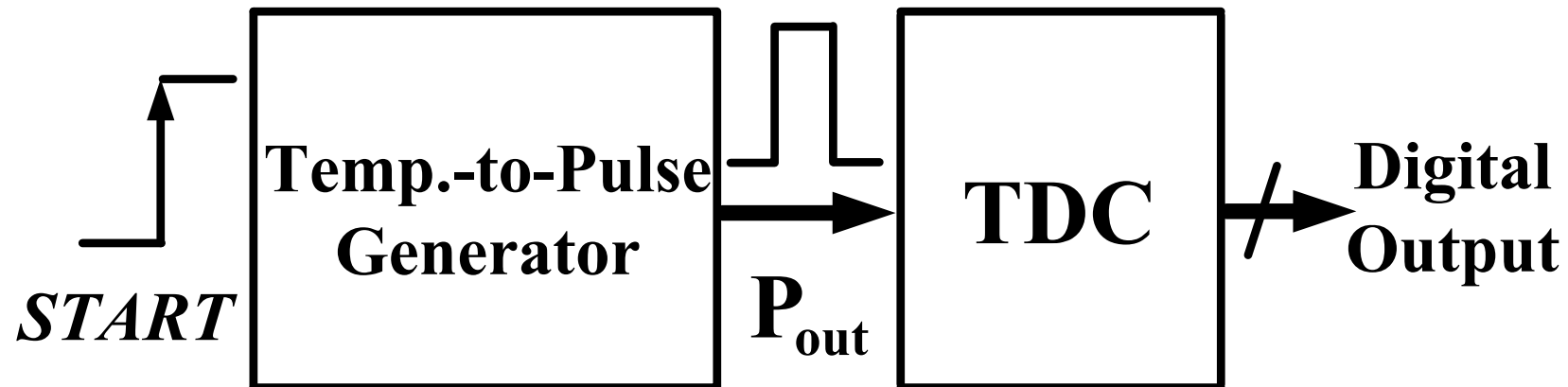
- $\pm 0.5^{\circ}\text{C}$ Accuracy over a Wide Temperature Range
- -55°C to $+125^{\circ}\text{C}$ Operating Range
- 2.7V to 5.5V or 1.7V to 3.7V (DS620) Supply Range
- User-Selectable 9- to 12-Bit Resolution
- No External Components Required to Measure Temperature
- Thermostat/Alarm Functionality with User-Defined Nonvolatile Thresholds

Common Specifications

	Min	Max	Unit
Accuracy	0.3	3	°C
Resolution	0.05	1	°C
Supply Voltage	2.5	5	V
Supply current	50	500	μA
Speed	1	50	Samples/s

Why Time-Domain?

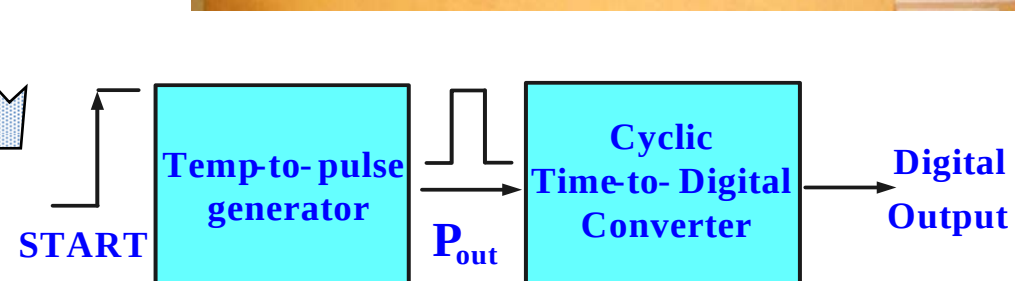
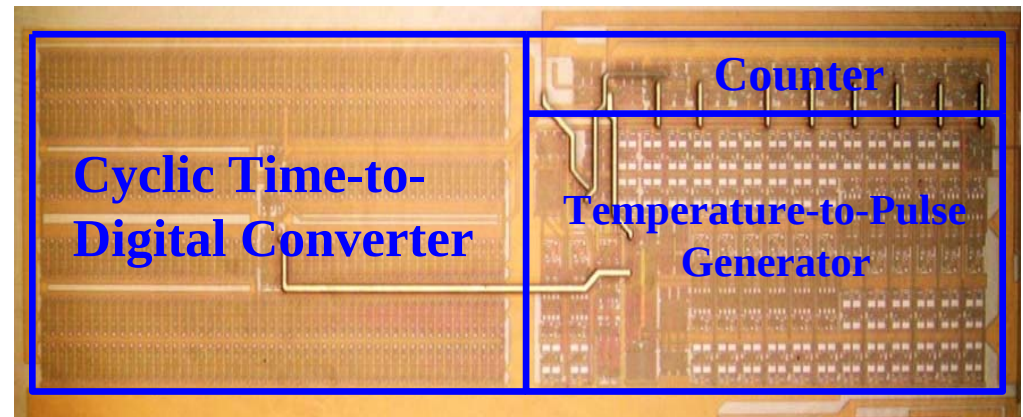
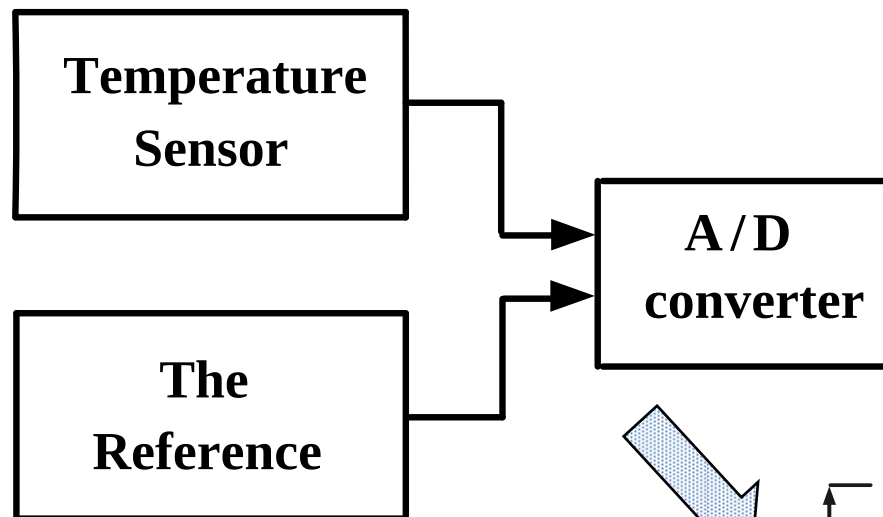
- reduce cost
- eliminate the burden of the curvature calibration
- No BJT used
- Convert temperature into time instead of V/I
- TDC instead of ADC used



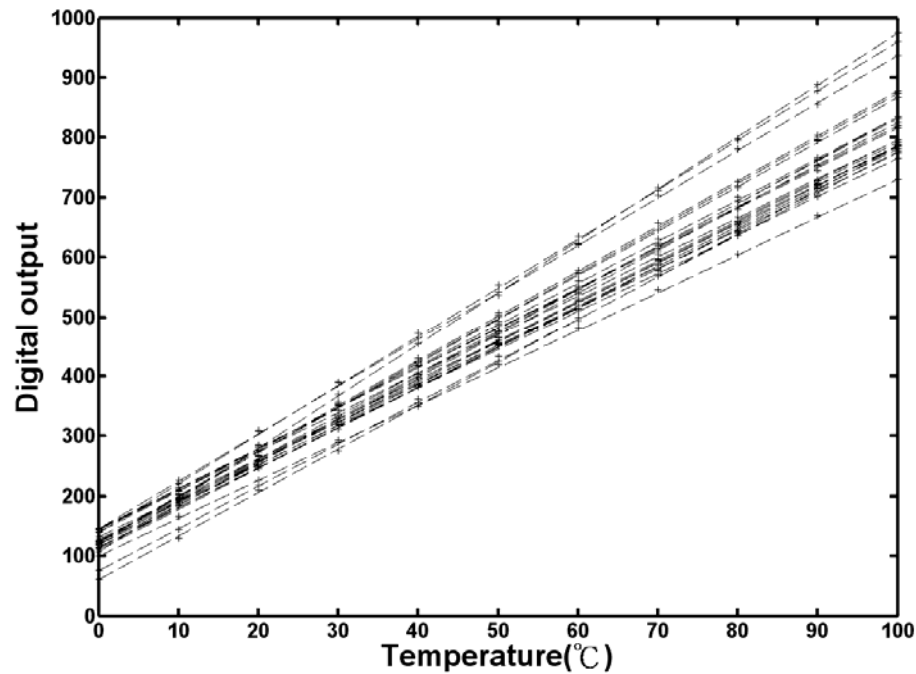
Time-domain Smart Temperature Sensor

P. Chen, JSSC 2005

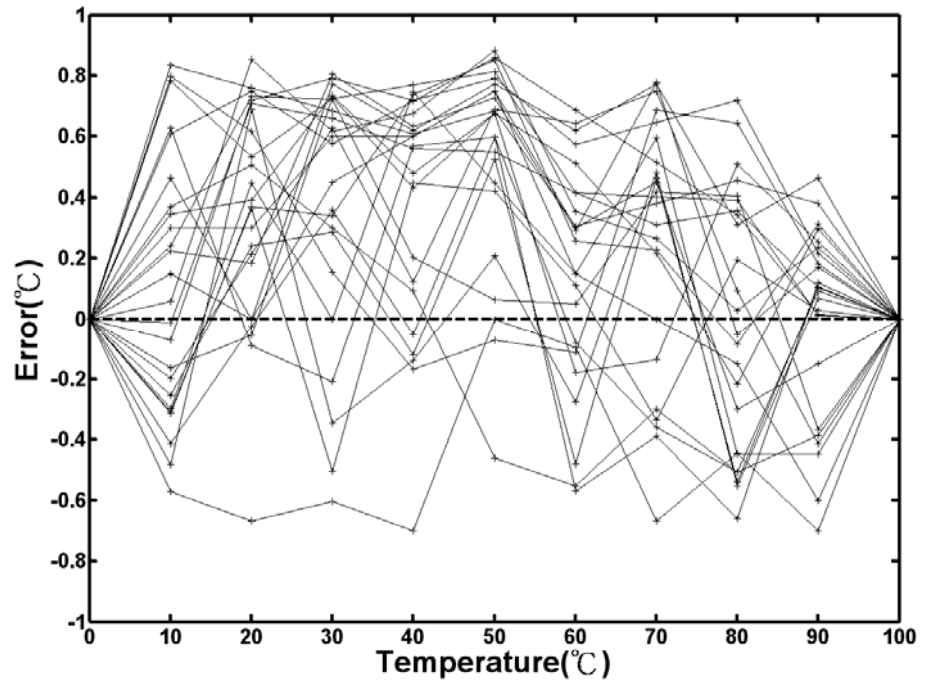
- First chip based on TDC
- TDDL delay > TRDL delay
- LSB=0.16°C, INL=-0.7~0.9°C
- 0.175mm², 10μW @ 10μW 2 samples/s



Measurement Results



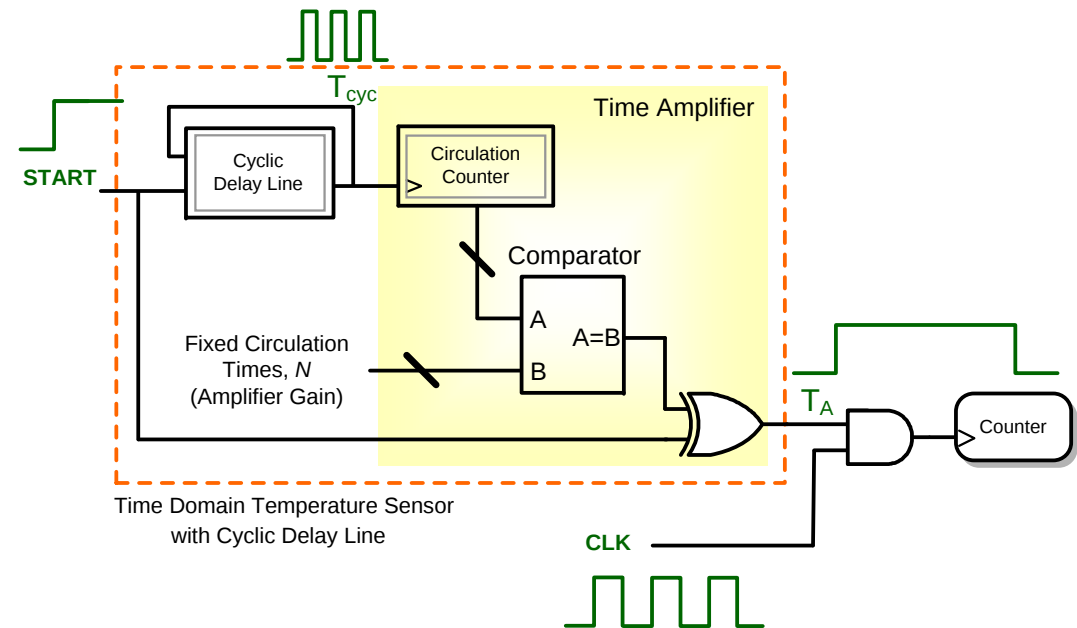
measurement results of 25 test chips



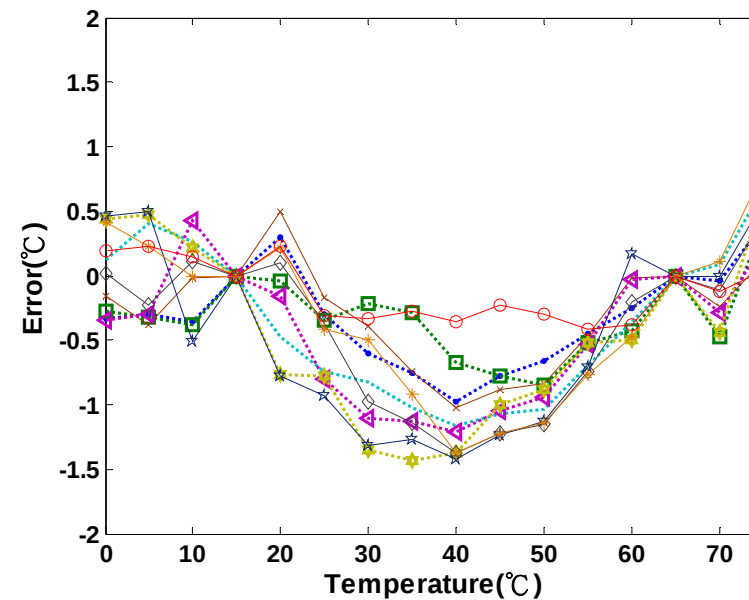
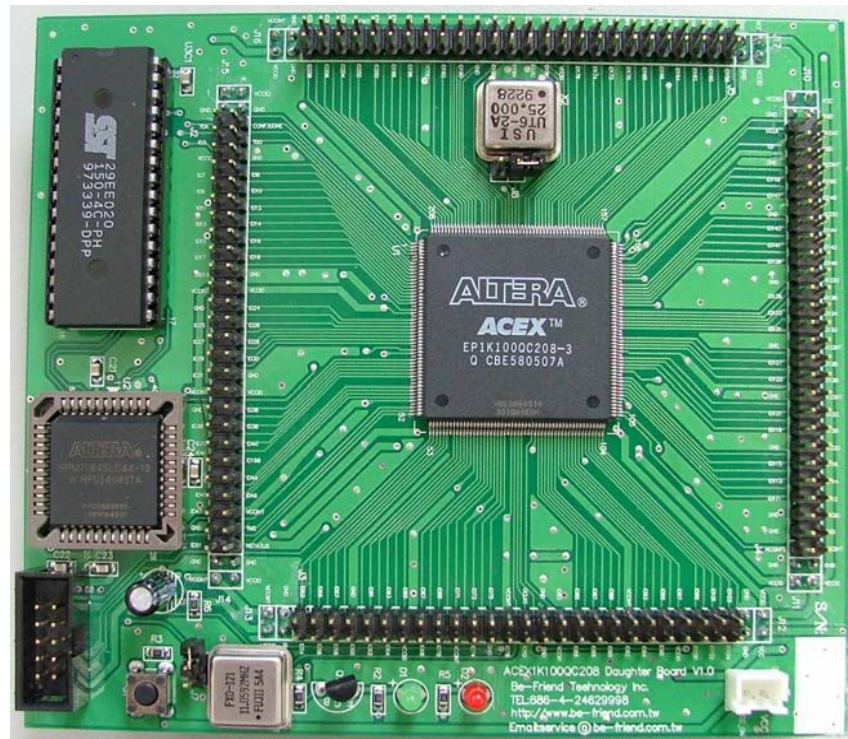
Error after 2-point calibration

FPGA Smart Temperature Sensor

- First FPGA thermal sensor
- Pure cell-based design
- Only 140 LEs used
- INL Error: $-1.5 \sim 0.8^{\circ}\text{C}$ for $0 \sim 75^{\circ}\text{C}$ range
- Power: $8.4\mu\text{W}$
- 70-LE version under measurement



Prototype & Result



Effective measurement errors of 10 FPGA chips with two- temperature calibration

P. Chen, TCAS-I 2007