The Innovative Analog Applications of FPGA

Poki-Chen

Ananlog IC LAB, ET, NTUST

Introduction

- Speaker: Associate Prof. Poki Chen
  - Associate Editor, IEEE TVLSI Syst.
  - Director of SoC Research Center, NTUST
- Room: EE807-2 Electronics Engineering Building, NTUST
- Email: poki@mail.ntust.edu.tw
- Website: http://homepage.ntust.edu.tw/poki/
- Majors
  - Analog and mixed-mode IC design & layout
  - Time-domain signal processing circuits
  - FPGA-based analog applications

2009 THE-QS Rankings

- Overall: Ranked 351 in the world (QS THES)
- Ranked 72 in Asia 400 / 2009

台灣各大學

2009年泰晤士報世界大學前400名排名

學校名稱	全球排名
台大	95
清大	223
成大	281
陽明	306
台科大	351
交大	389

製表：記者胡清暉

Analog IC Lab Members

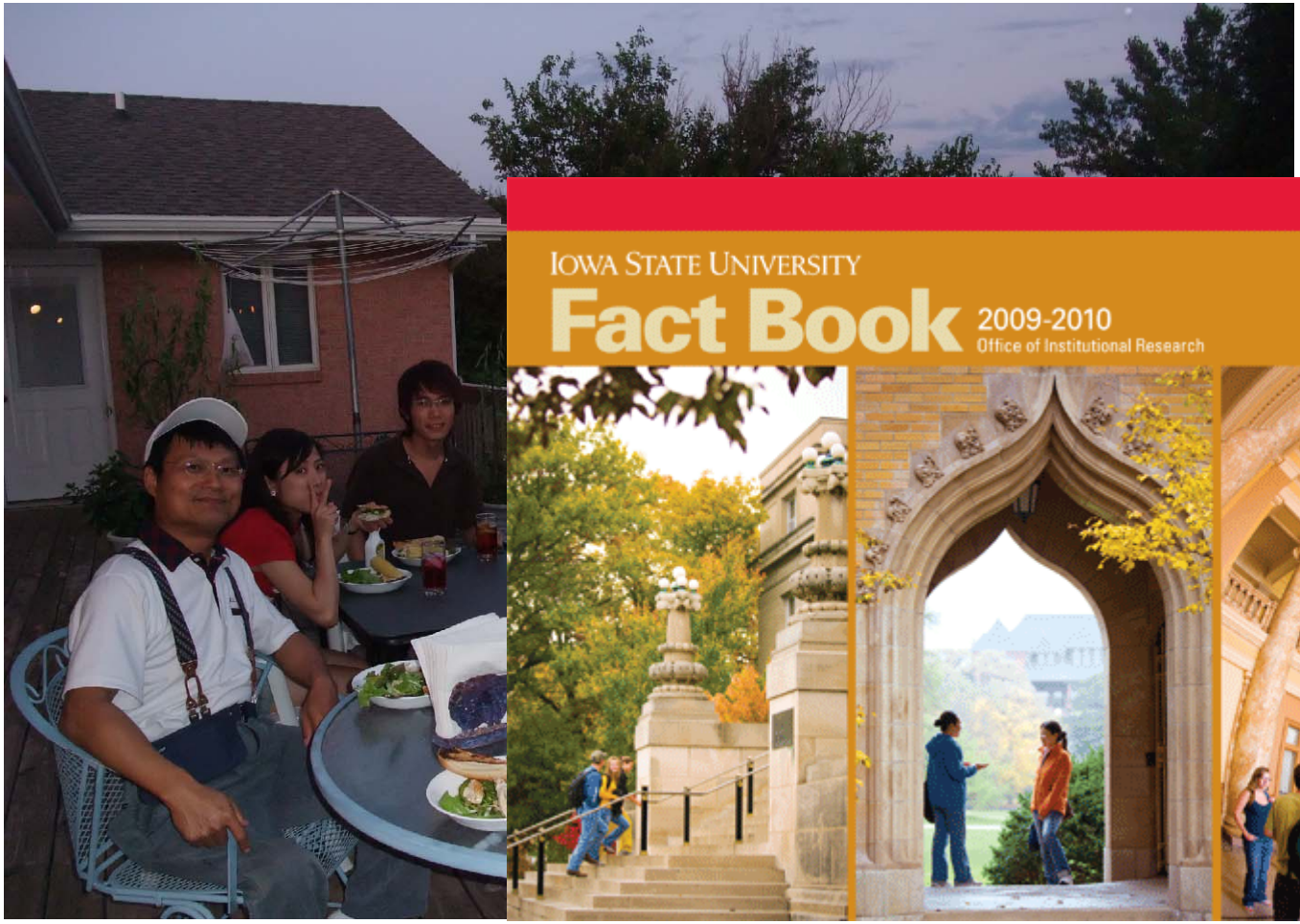
- **Laboratory Aims ：**
  - **Focused on mixed-mode IC design**
  - **Excellent paper, patent, IP, and well-trained engineers**
- **Laboratory members ：**
  - **Doctor of Philosophy (PH.D.) : 2**
  - **Master : 9**
  - **Bachelor : 7**
  - **hard-working much required**

The LAB racing with Time


Research Opportunities and Challenges in


Research Opportunities and Challenges in Analog/Mi

ISU Visit !



IOWA STATE UNIVERSITY
Fact Book
2009-2010
Office of Institutional Research

ISU Visit ?

Delft Univ. of Tech. Visit

Guidelines

- Motivation
- FPGA Time-to-Digital Converter
- FPGA Digital-to-Time Converter
- FPGA Time-Domain Smart Temperature Sensor
- Future Research Topics

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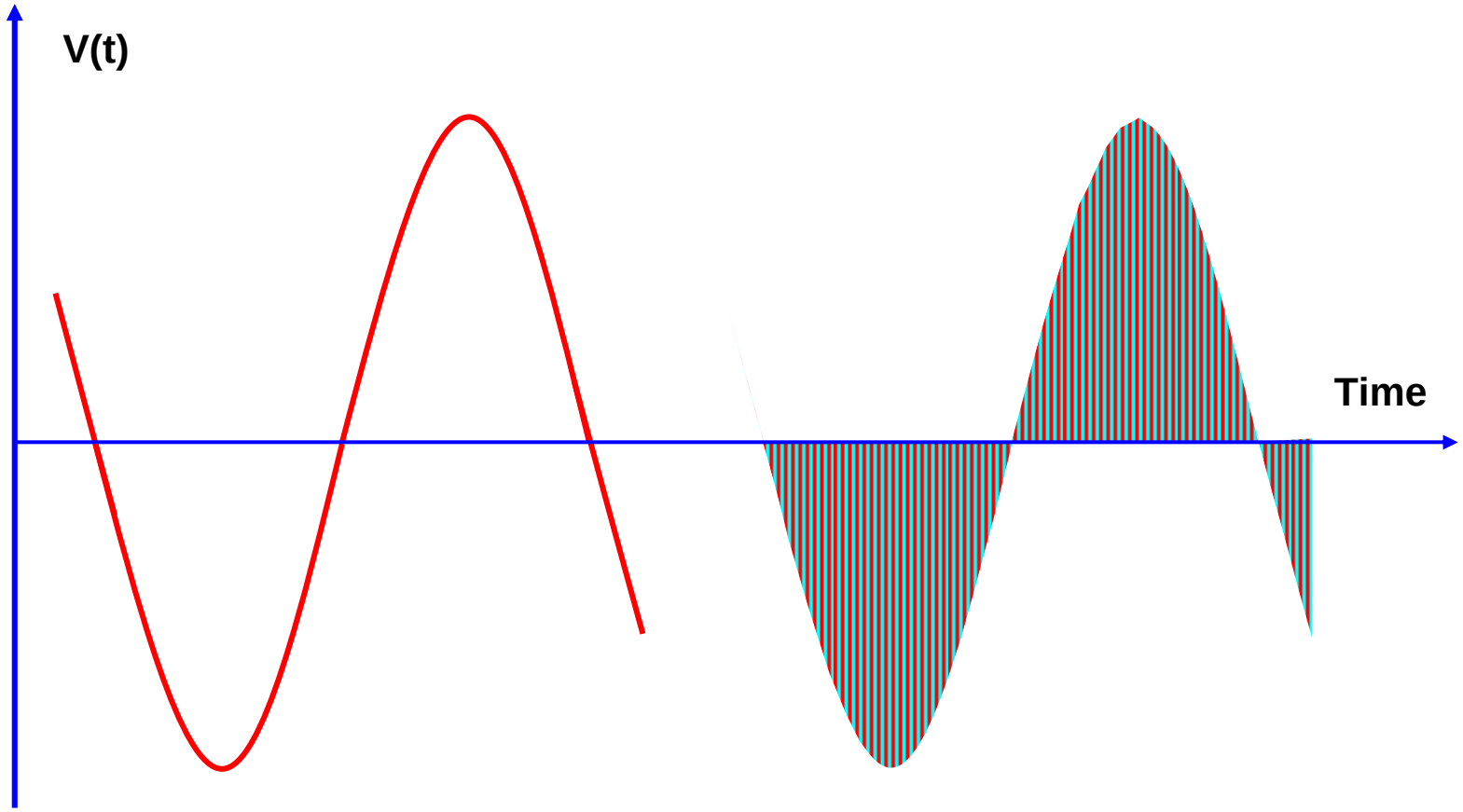
Analog vs. Digital



Analog signal

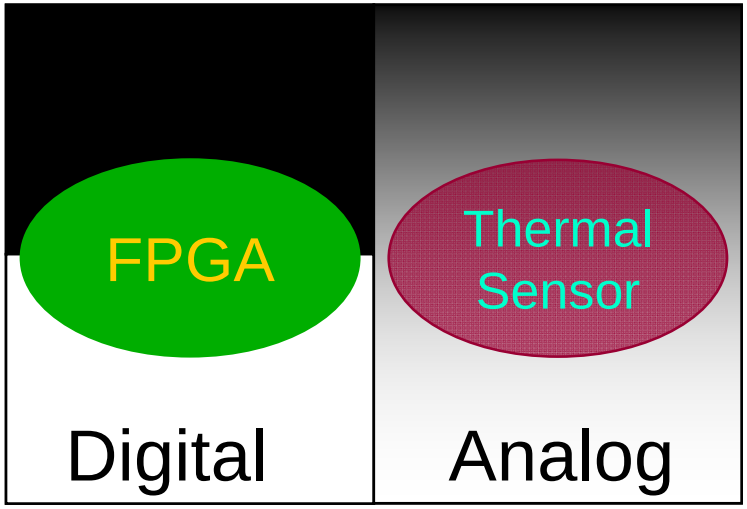
Digitized signal

Analogue versus Digital

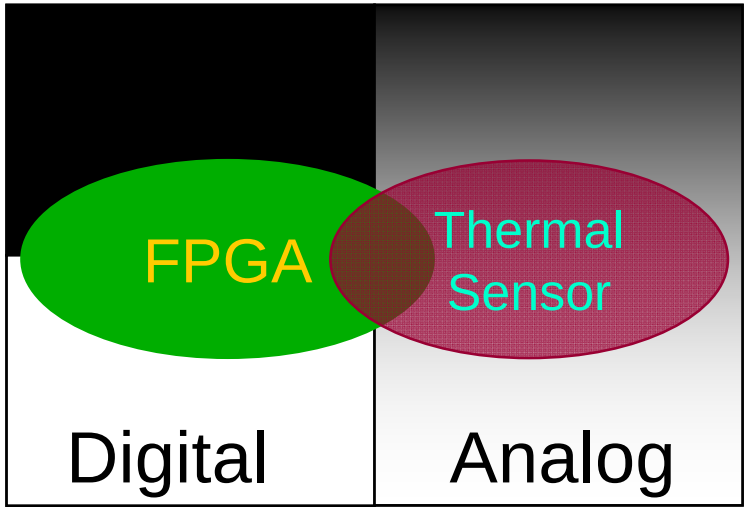
	Analog Design	Digital Design
Signal	Continuous	Discrete
Design	Customized	Standardized
Model requirement	Precise model	Abstract model
Programmability	Hard to change	Programmable by software
Design level	Circuit level	System level
CAD tools	Difficult to use with CAD tools	Amenable to CAD tools
Complexity	Too many deign parameters	Simple and easy

Why FPGA

- Fast prototyping
- Easy to port among processes
- Compatible to cell-based design
- More and more built-in analogue blocks



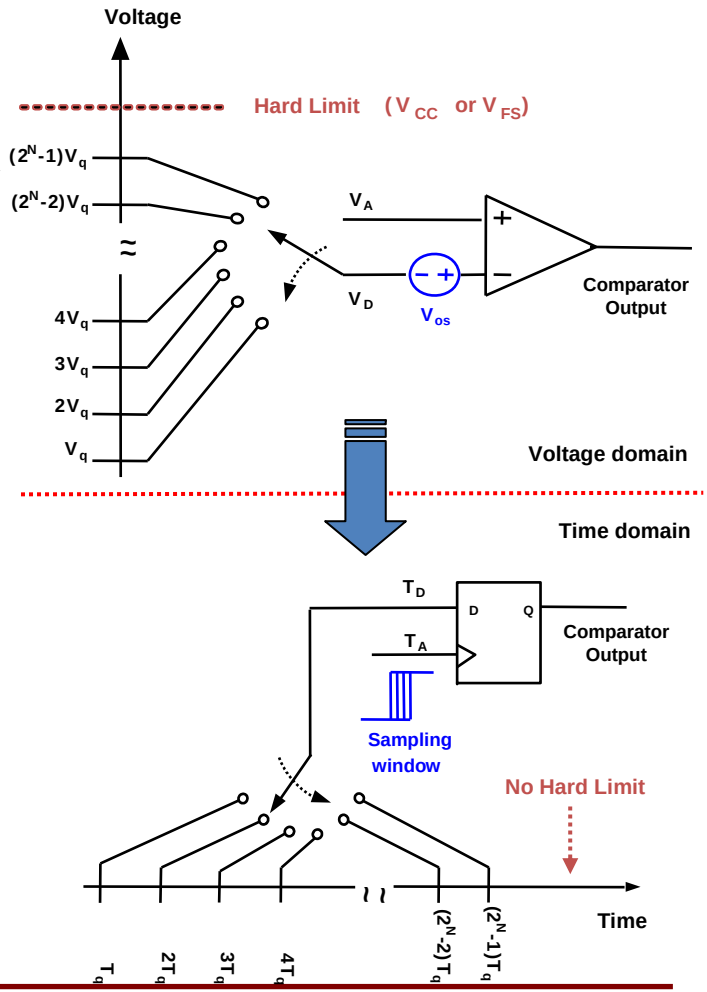
Conventional distribution



Current distribution

Why Time-Domain?

- Supply voltage scalable with process
- Smaller sampling window (dead zone)
- No hard limit for operation range
- Simpler circuit
- Lower chip size and cost
- Possible to digitize circuit



- Motivation
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- FPGA Digital-to-Time Converter
- FPGA Time-Domain Smart Temperature Sensor
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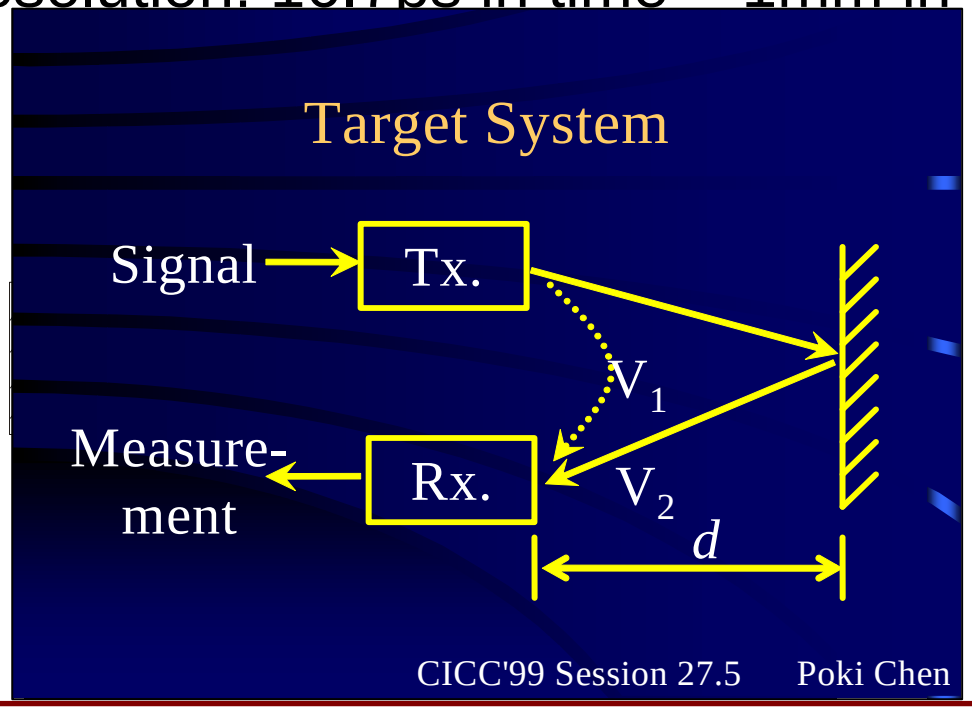
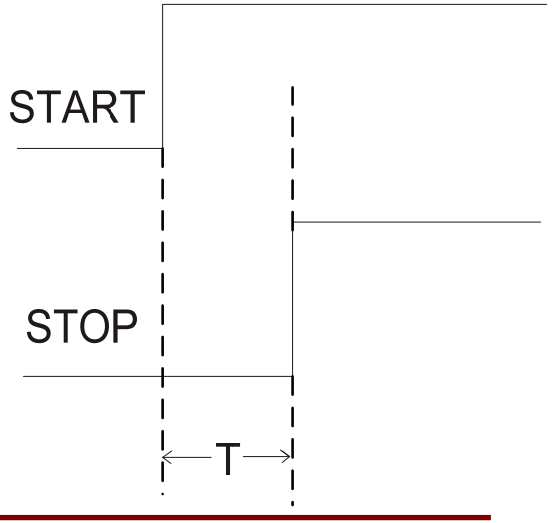
Applications

- Particle detection for high energy physics
- Phase Demodulation
- Laser ranger
  - Resolution: 16.7ps in time ~ 1mm in distance
- …..



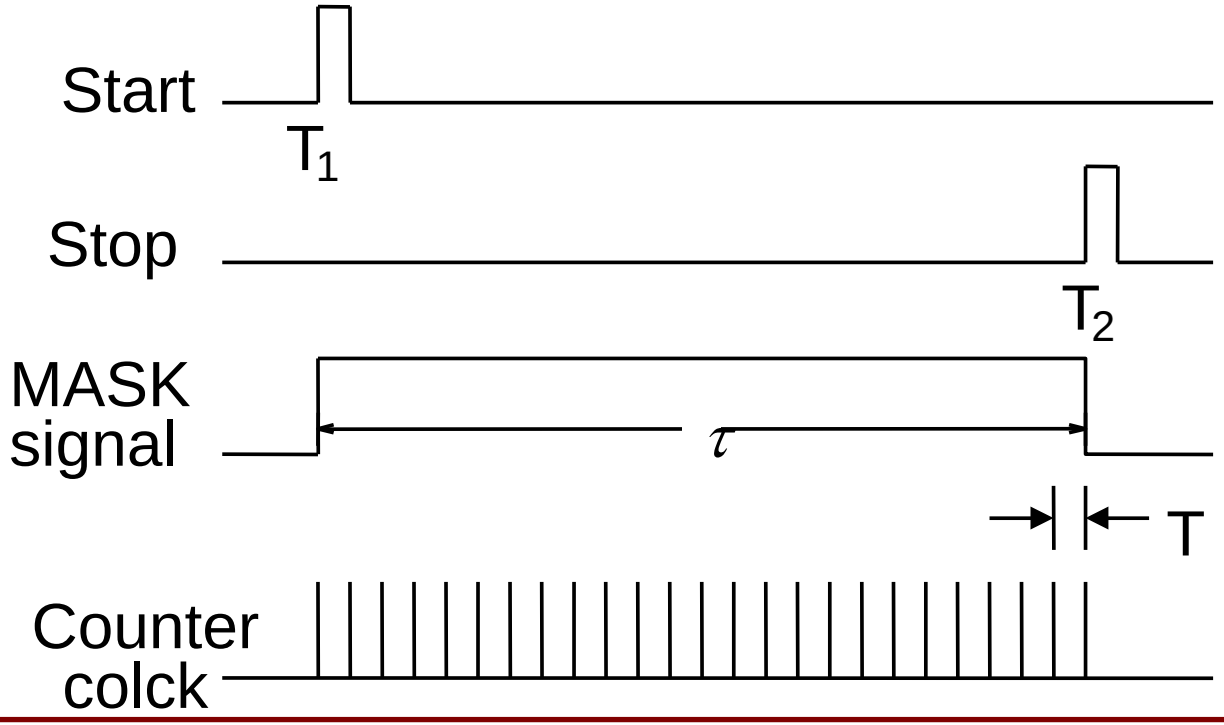


Brief History

- ECL versions
  - Large PCB, high power
- CMOS TDC (1995, JSSC)
  - LSB=780ns, power=15mW
  - single-shot accuracy=3ns
- FPGA TDC (1997, IM)
  - LSB=200ns
  - Trial-and-error realization
- CMOS TDC with cyclic delay line (1997,EL)
  - LSB=286ps
- New pulse-shrinking delay element (1999,CICC)
  - LSB=68ps

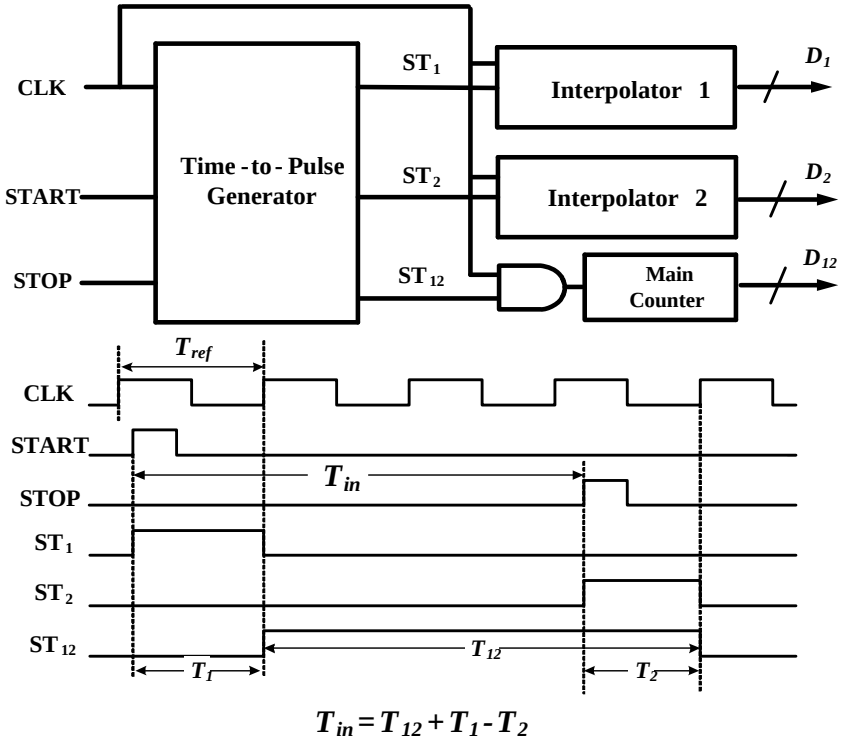
Counter-Based TDC

- Excellent linearity but with poor resolution
- Synchronization problem at both ends



Interpolation Circuit for TDC

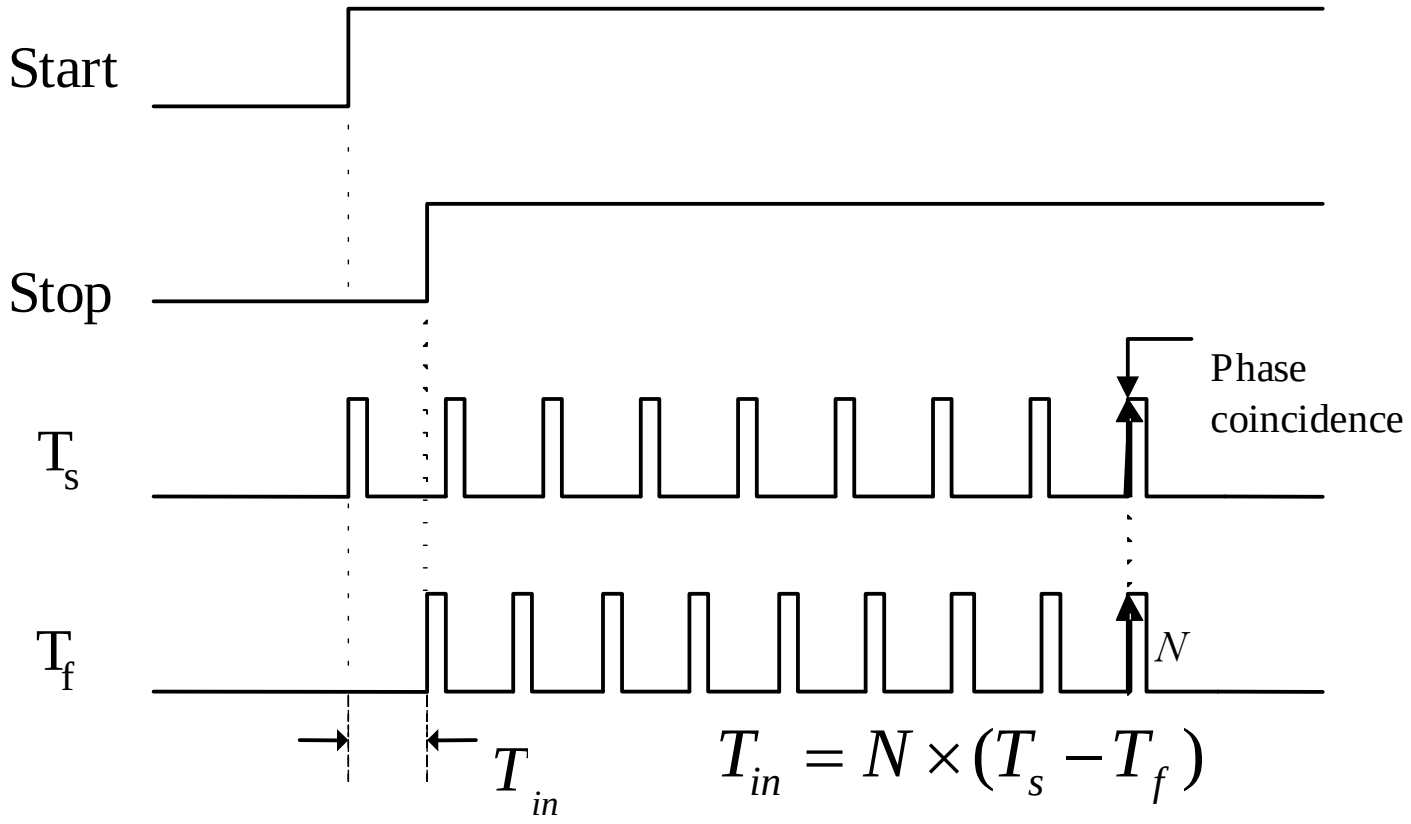
- Resolve fractional periods at both ends
- Error caused by mismatch between main & interpolation circuits



$$T_{in} = T_{12} + T_1 - T_2$$

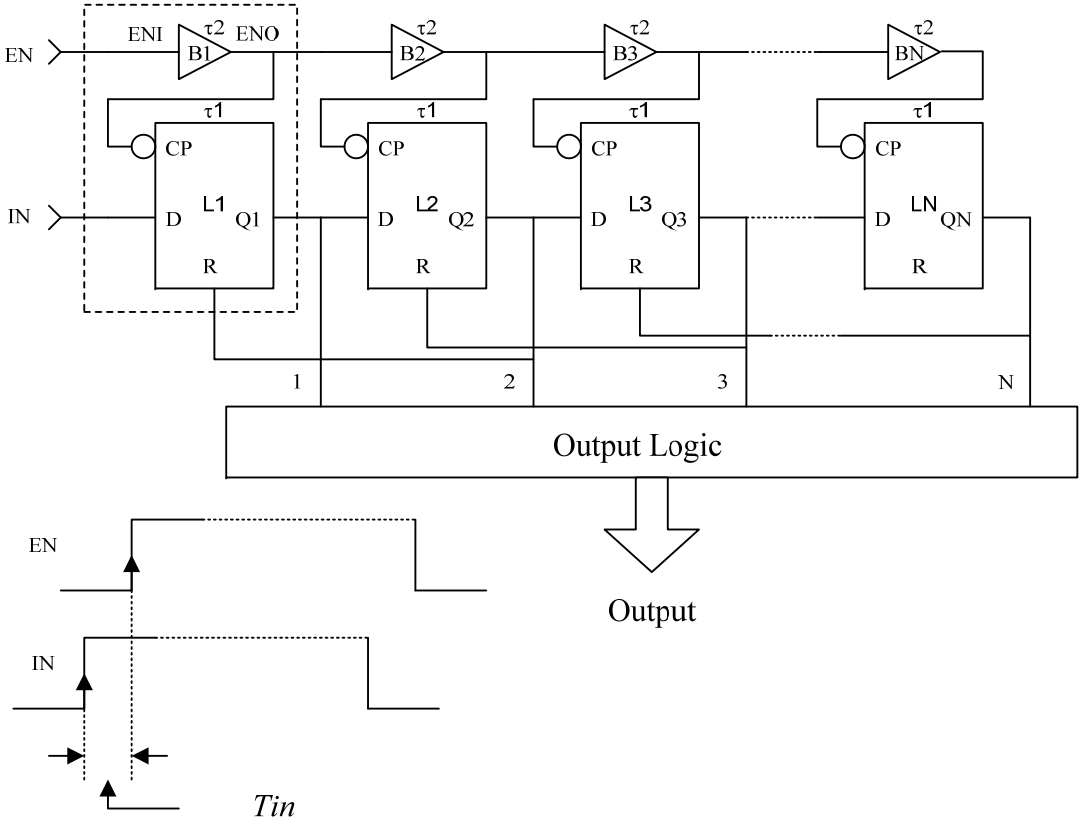
Vernier Principle

- Resolution = period difference

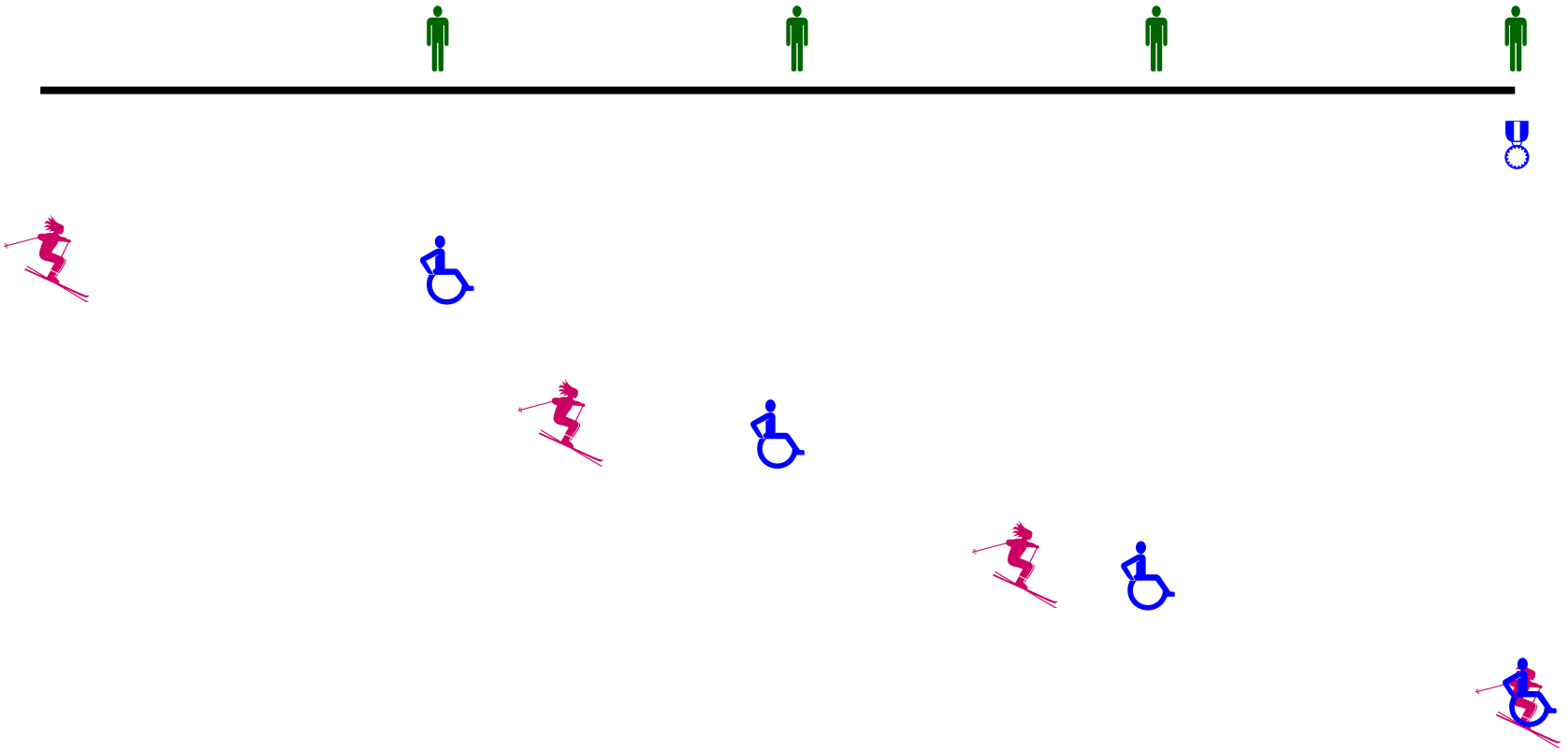


First FPGA TDC

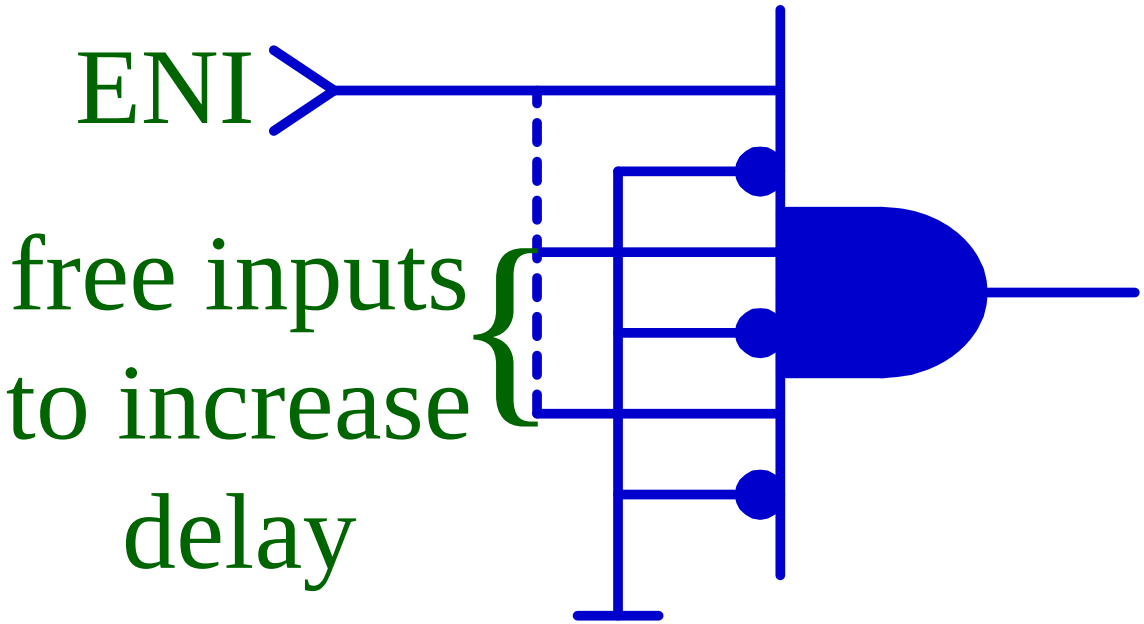
- Based on vernier principle
- Trial-and-error design with QuickLogic pASIC FPGA



Racing in Line



- Delay controlled by input pins connected



- LSB=200ps
- 20ps resolution achieved in my Lab

J. Kalisz, IM 1997

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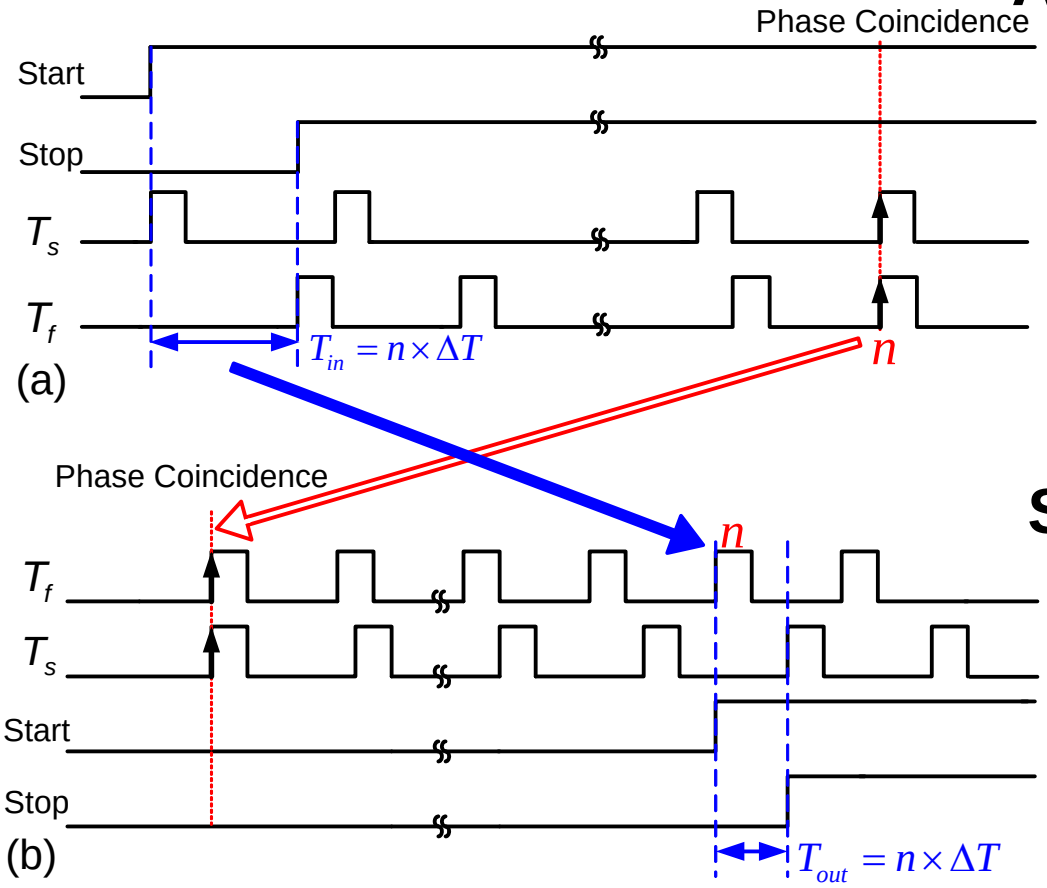
- FPGA Time-to-Digital Converter
- FPGA Digital-to-Time Converter
- FPGA Time-Domain Smart Temperature Sensor
- Future Research Topics

Operation Principle: From TDC to DTC



At phase coincidence,

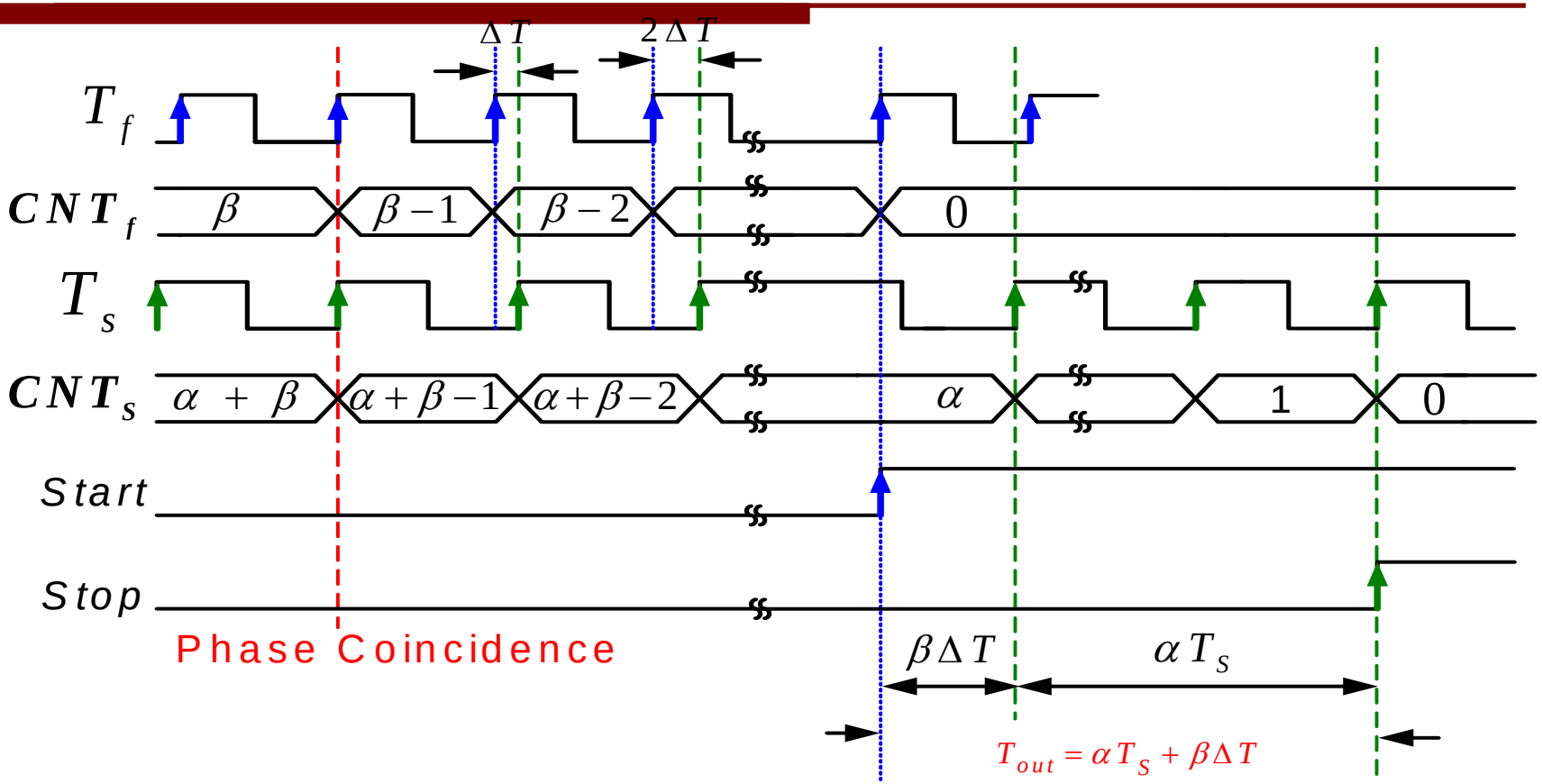
$$T_{in} = n\Delta T \quad \textbf{(1)}$$

Similarly,

$$T_{out} = n\Delta T \quad \textbf{(2)}$$

Fig. 1 (a) The vernier TDC, (b) the proposed vernier DTC

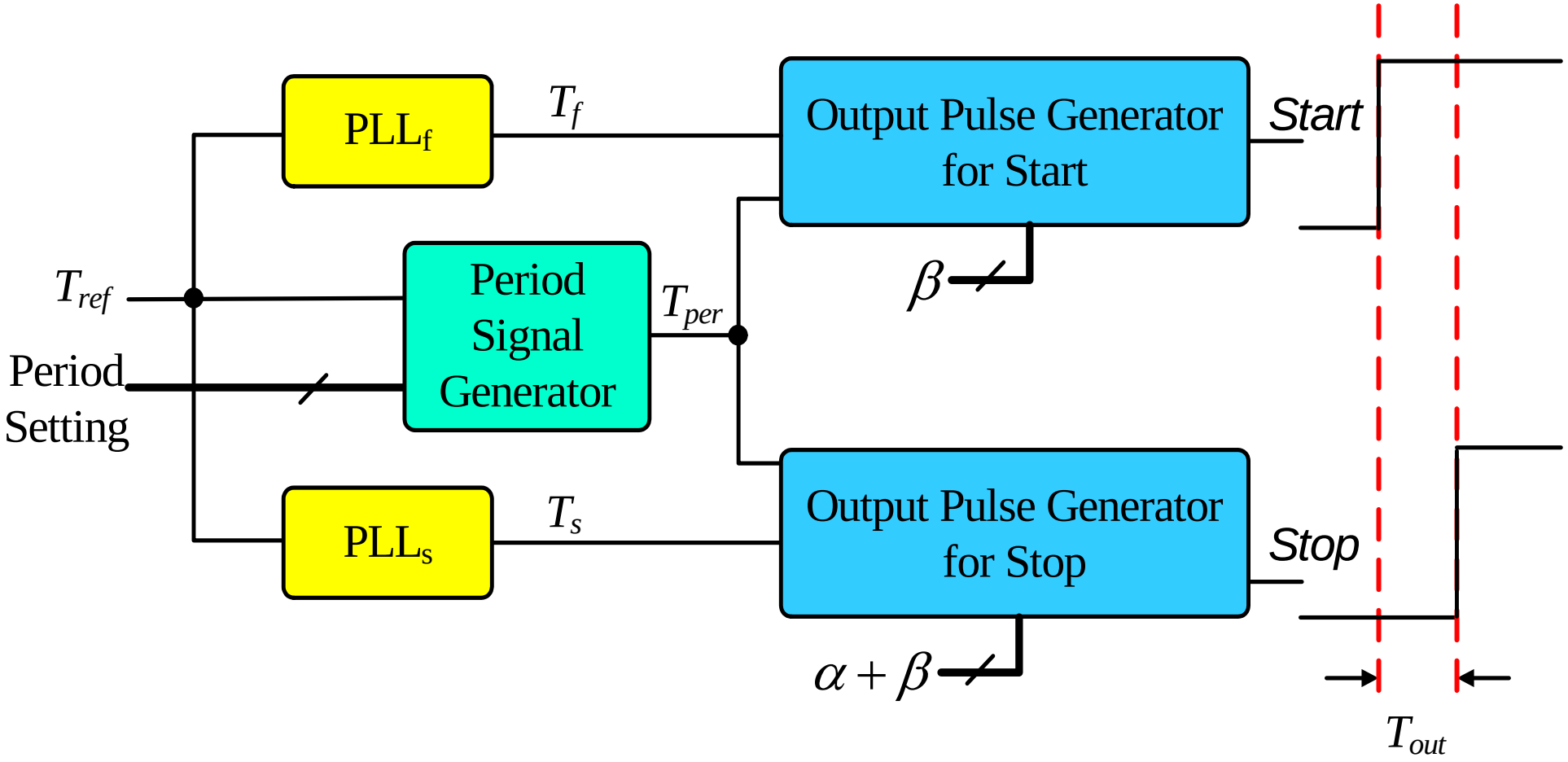
Operation Range Extension with Less Latency



The width of output signal becomes

$$T_{out} = (\alpha+\beta)T_s - \beta T_f = \alpha T_s + \beta(T_s - T_f) = \alpha T_s + \beta \Delta T \qquad \textbf{(4)}$$

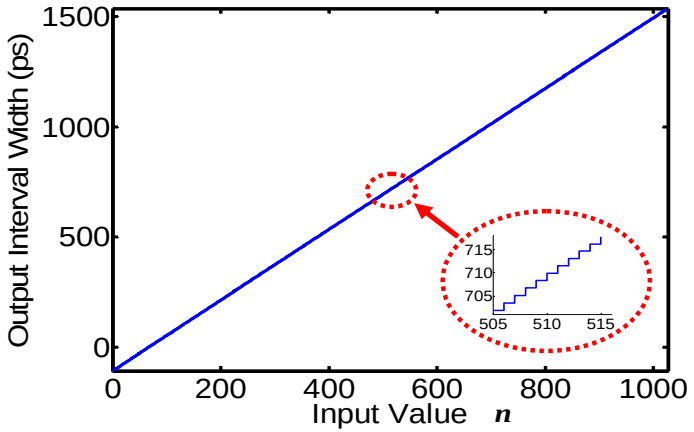
Block Diagram

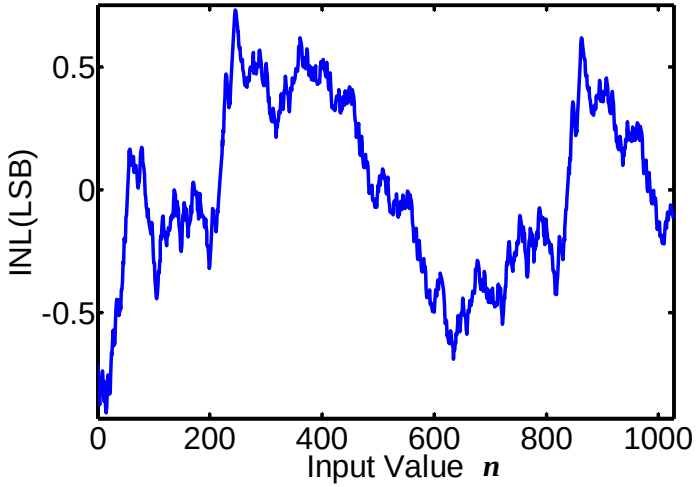


P. Chen, TCAS-I 2010

FPGA Digital-to-Time Converter

- Xilinx Vertex IV
  - Resolution: 35ps
  - Error: ±7 ps
- Atera Stratix III
  - Resolution= 1.58ps
  - Error: -0.25~+0.3 ps
- Tsao's paper
  - Resolution: 37.5ps
  - Error~260ps
- Agilent Pulse Generator 81130A
  - Resolution: 2ps
  - Error >100ps
  - List price: US$ 23k

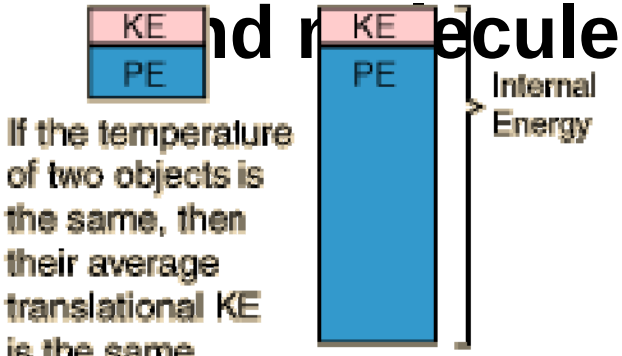




- Motivation
- FPGA time-to-digital converter
- FPGA Time-domain smart temperature sensor
- FPGA Digital-to-time converter
- Future Research Topics

What is temperature?

- **operational definition**
  - **a measure of the average translational kinetic energy associated with the disordered microscopic motion of atoms and molecules**



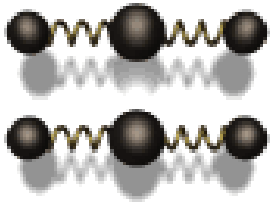
If the temperature of two objects is the same, then their average translational KE is the same.

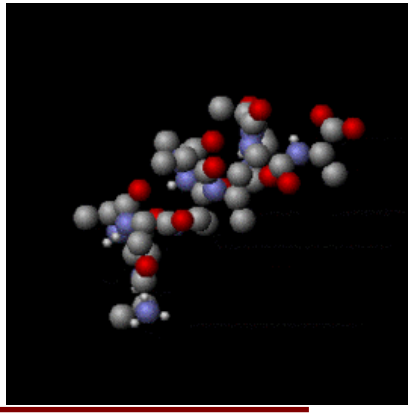
Their internal energies and specific heats will not necessarily be the same.

$$\left[\frac{1}{2}mv^2\right]_{average} = \frac{3}{2}kT$$

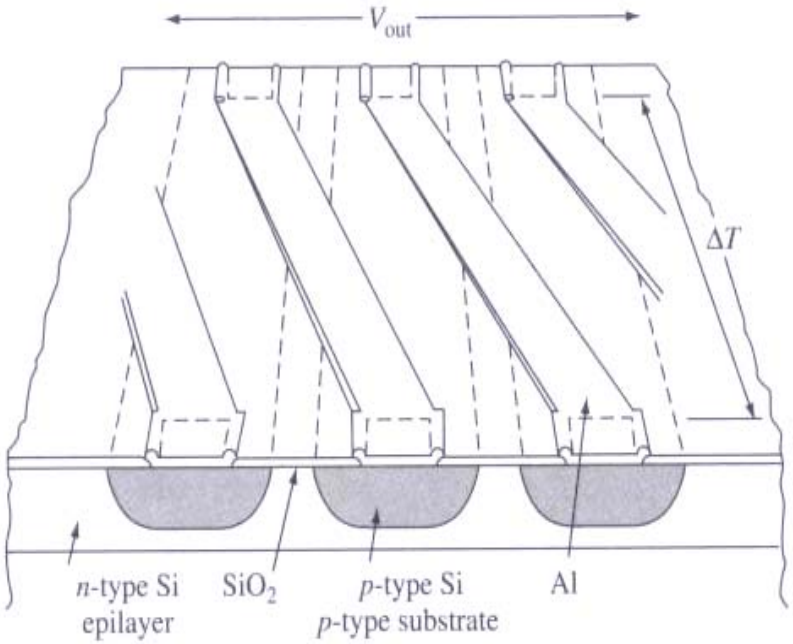
defines the kinetic temperature

k = Boltzmann constant



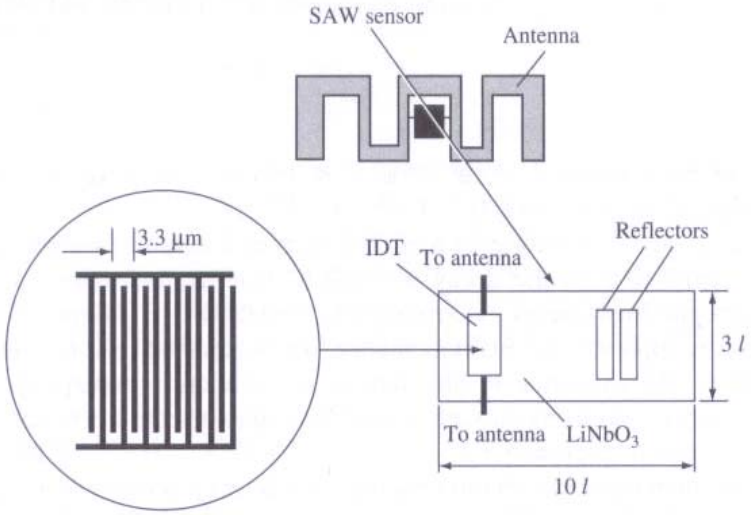


Thermistor



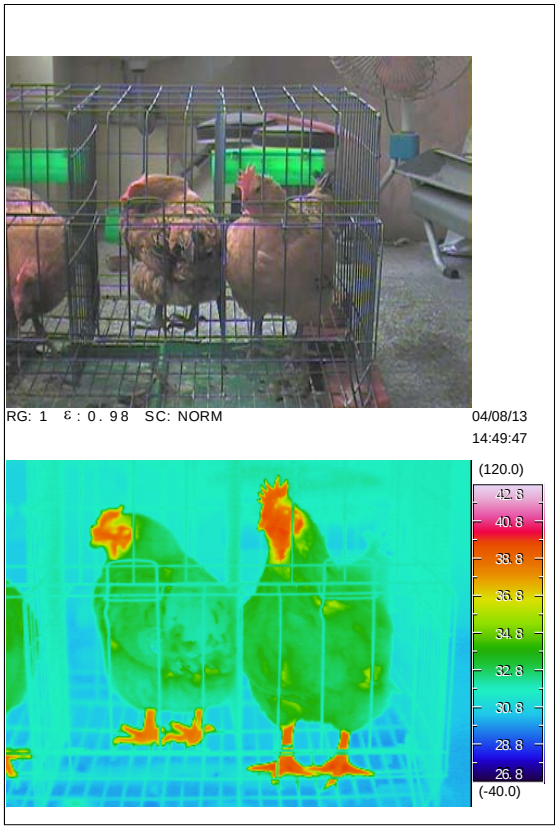
From: Meijer et al, 1994

Integrated passive SAW-IDT temperature

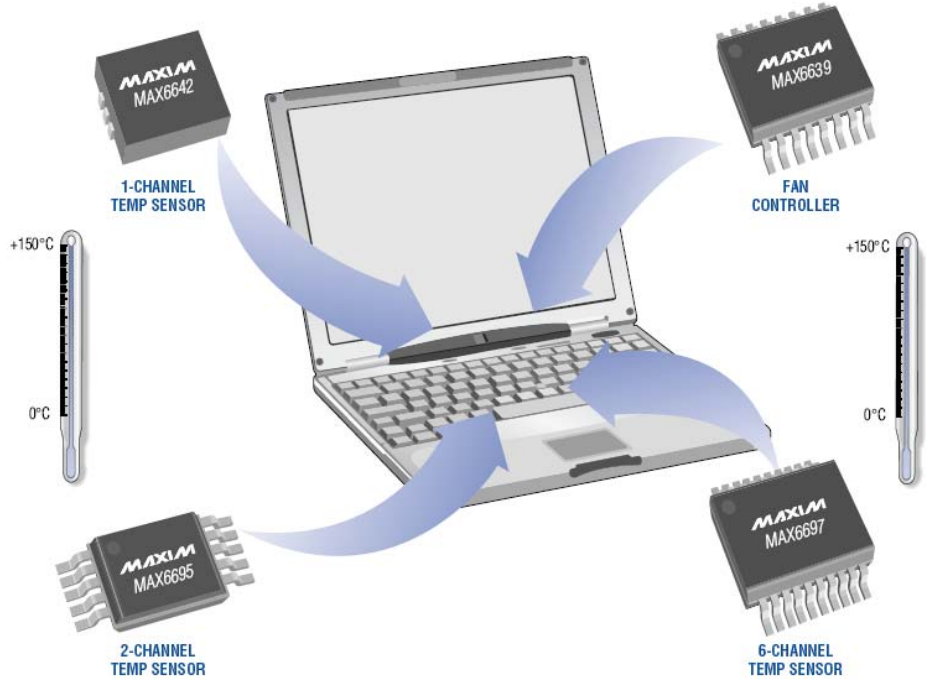


From: Bao et al, 1994

Applications

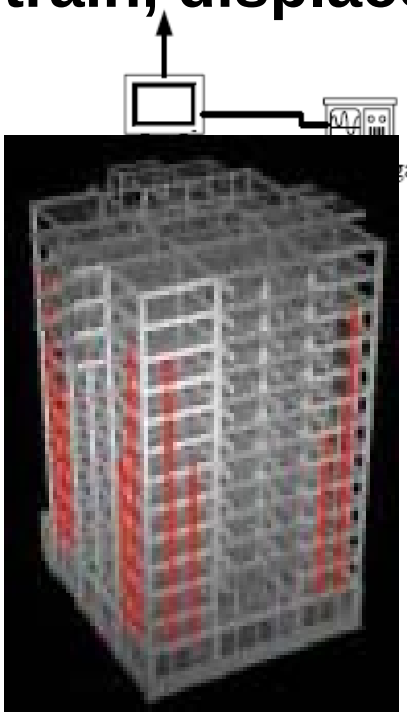


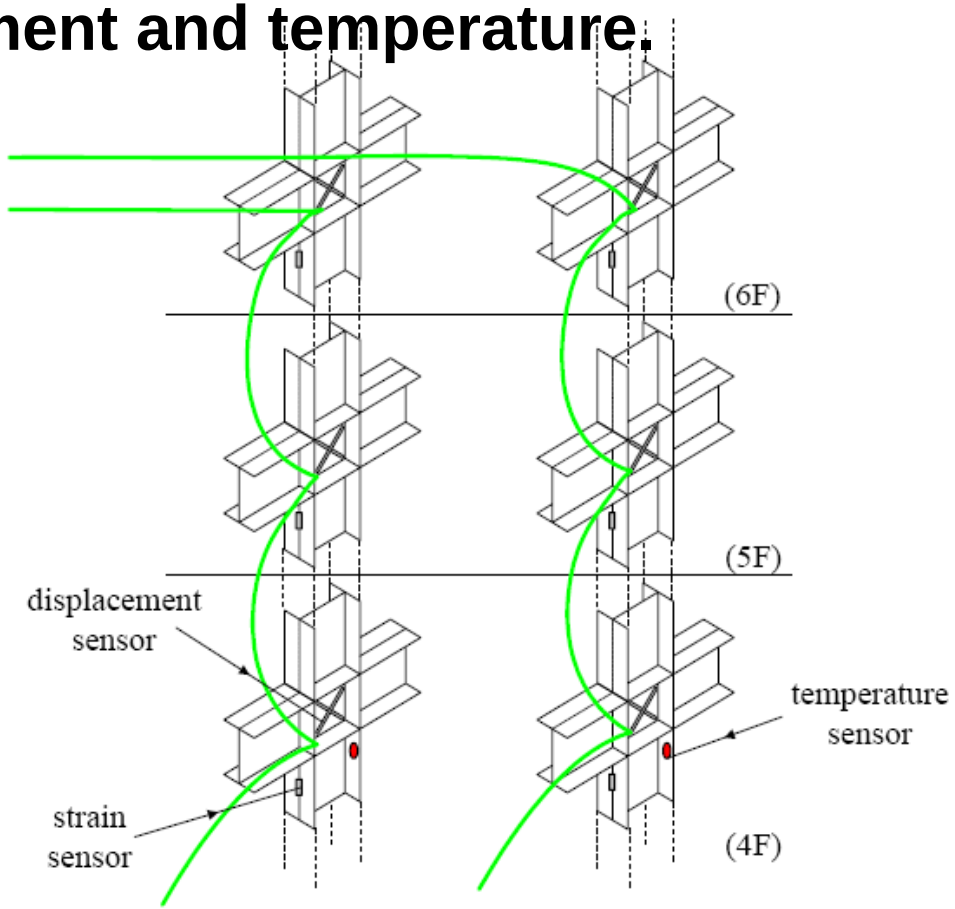
Digital Thermometer



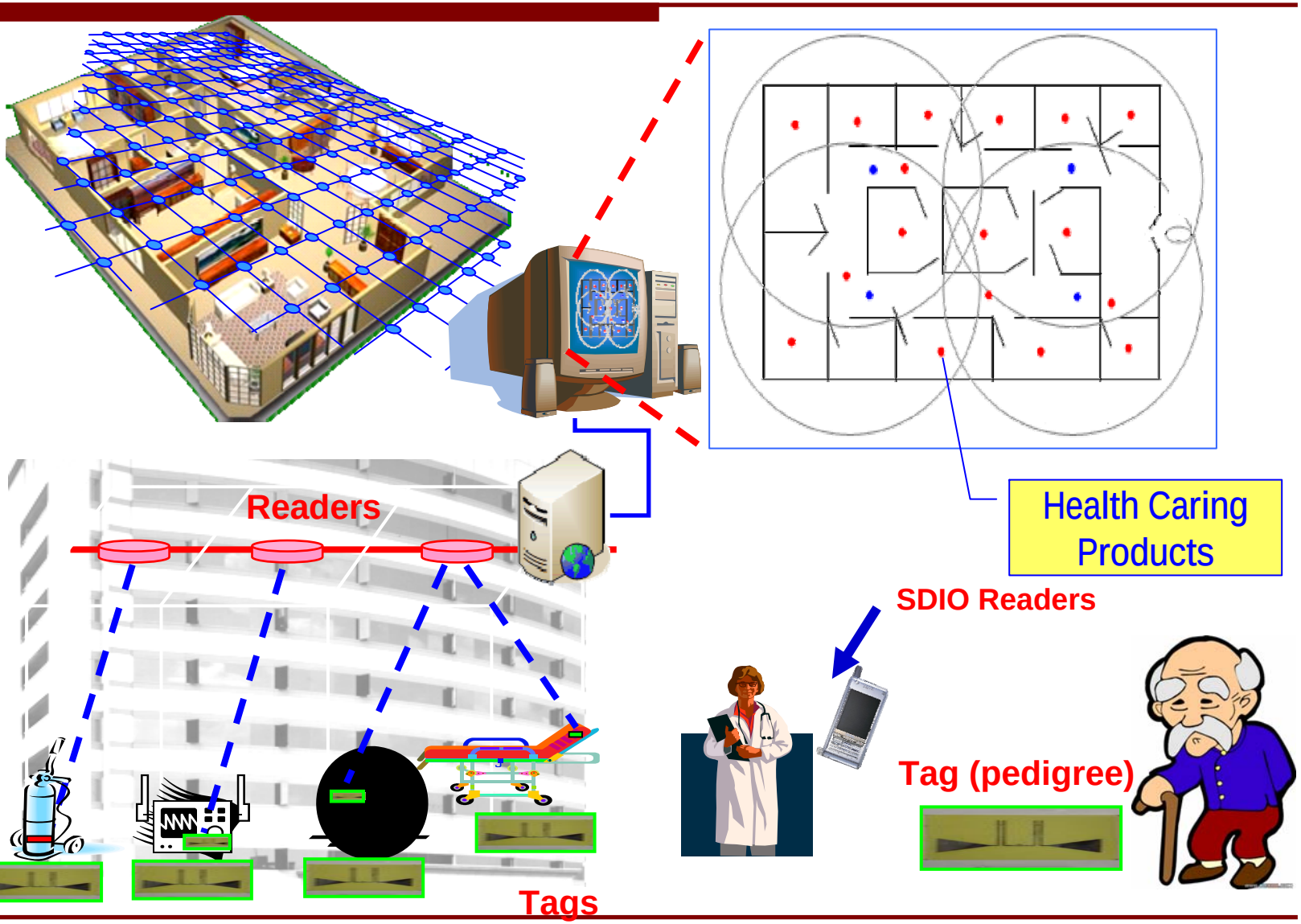
Structural Health Monitoring System

- ensure the structural integrity by monitoring the response of the building.
- measure strain, displacement and temperature.



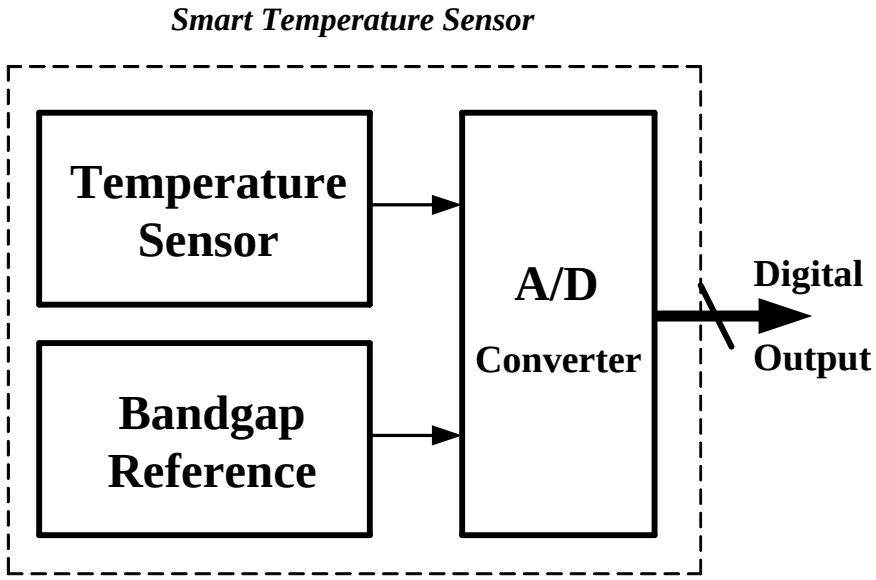


Body Sensor Network



Voltage-Domain Predecessors

- Parasitic BJT used
- Subtle calibration circuits adopted
  - chopping and dynamic element matching (DEM)
  - second-order curvature correction
  - offset cancellation
  - $\Delta\Sigma$ modulator
- High accuracy OPAMP with large number of input bits



Industry's Highest Accuracy Temp Sensors

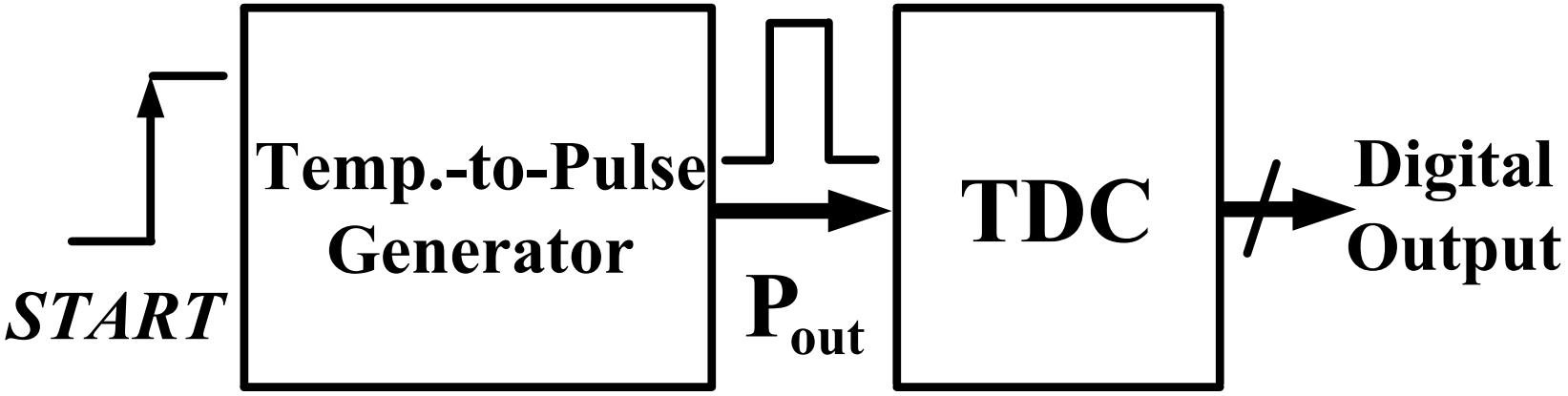
- ±0.5°C Accuracy over a Wide Temperature Range
- -55°C to +125°C Operating Range
- 2.7V to 5.5V or 1.7V to 3.7V (DS620) Supply Range
- User-Selectable 9- to 12-Bit Resolution
- No External Components Required to Measure Temperature
- Thermostat/Alarm Functionality with User-Defined Nonvolatile Thresholds

Common Specifications

	Min	Max	Unit
Accuracy	**0.3**	**3**	**°C**
Resolution	**0.05**	**1**	**°C**
Supply Voltage	**2.5**	**5**	**V**
Supply current	**50**	**500**	**μA**
Speed	**1**	**50**	**Samples/s**

Why Time-Domain?

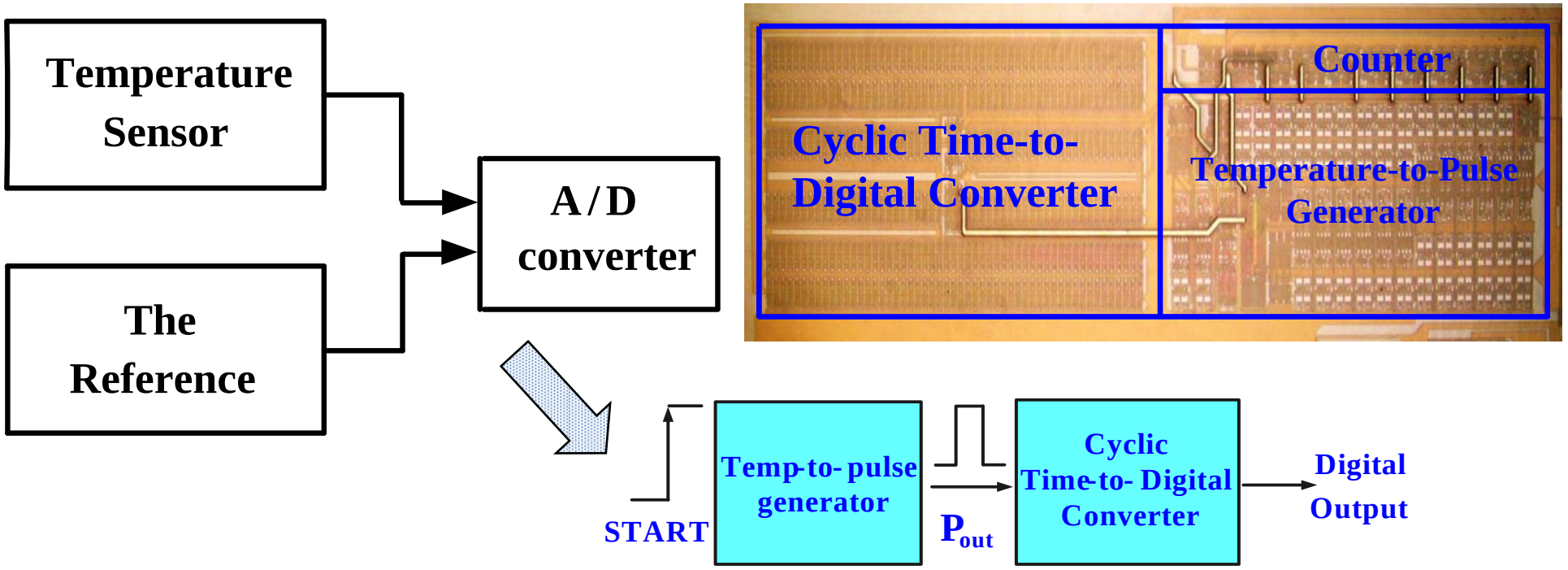
- reduce cost
- eliminate the burden of the curvature calibration
- No BJT used
- Convert temperature into time instead of V/I
- TDC instead of ADC used



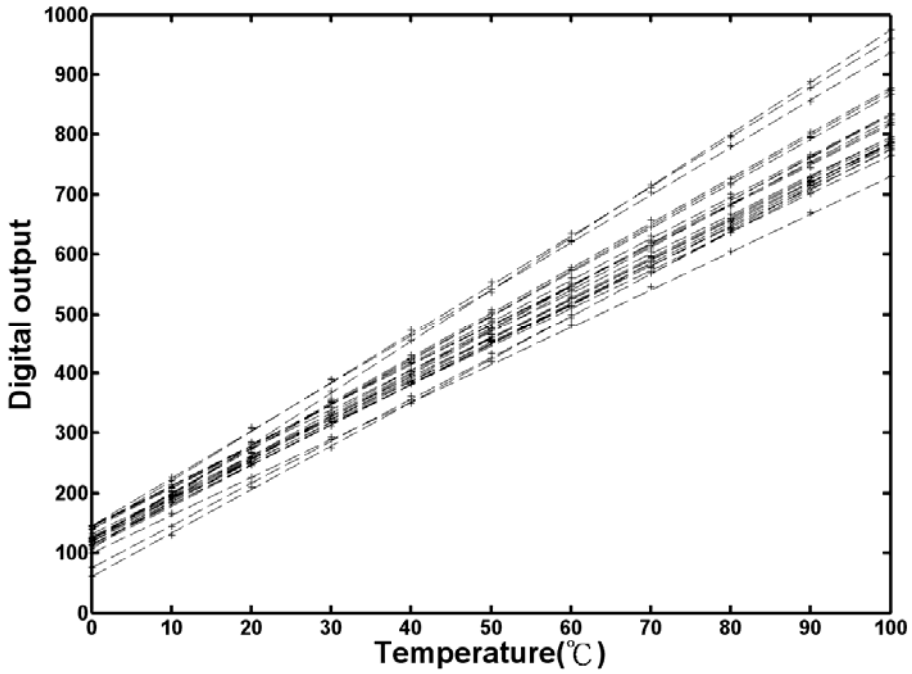
Time-domain Smart Temperature Sensor

P. Chen, JSSC 2005

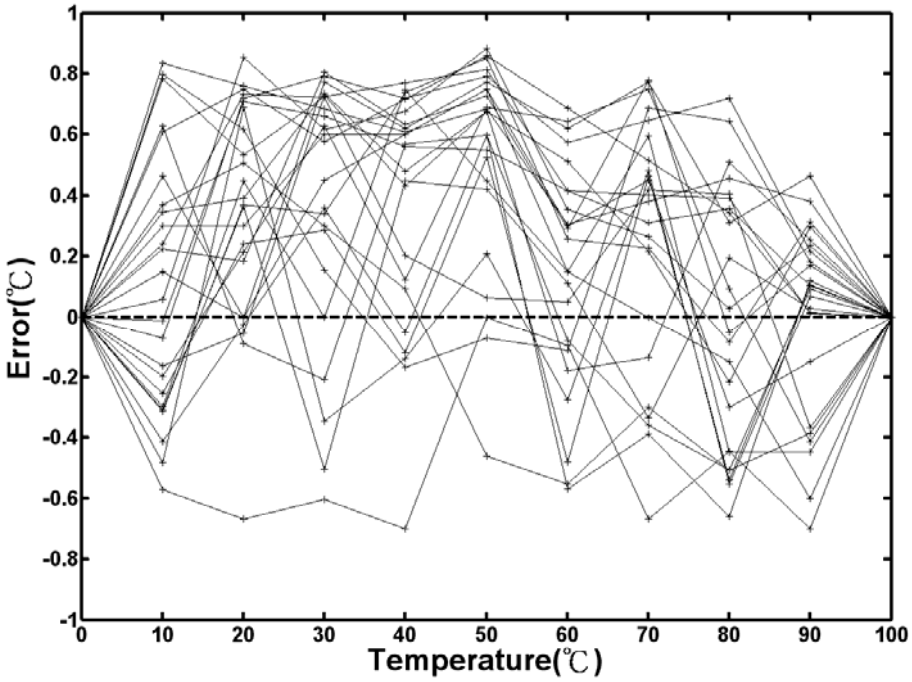
- First chip based on TDC
- TDDL delay > TRDL delay
- LSB=0.16°C, INL=-0.7~0.9°C
- 0.175*m*m², 10μW @ 10μW 2 samples/s



Measurement Results



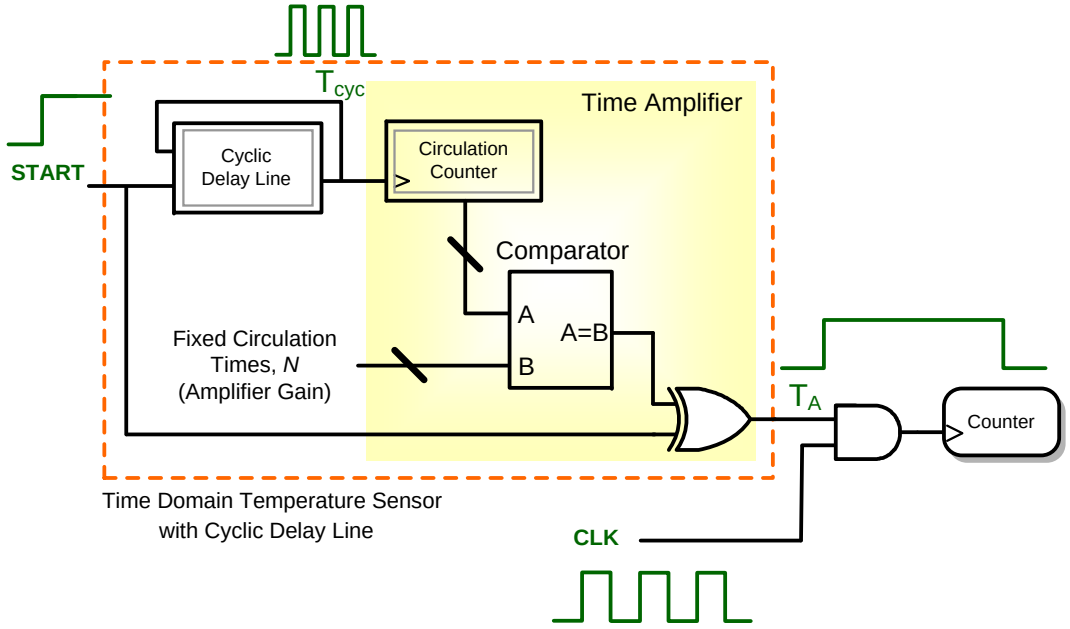
measurement results of 25 test chips



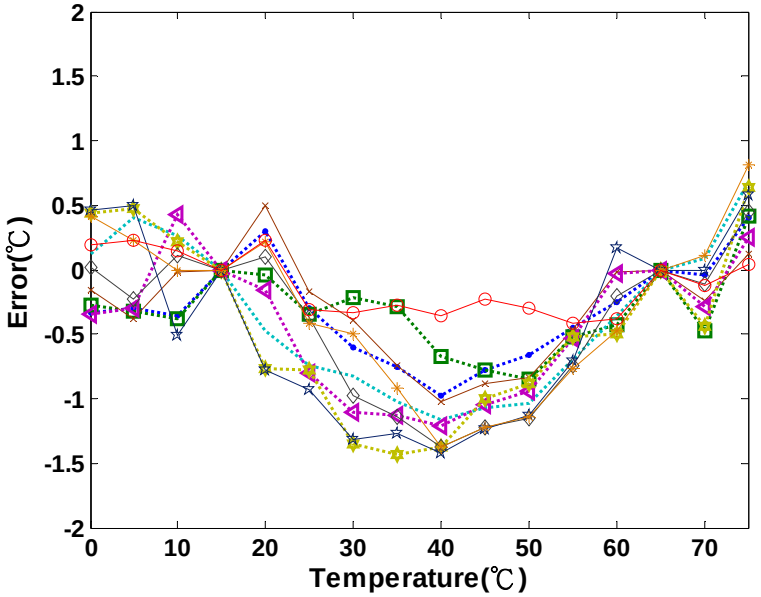
Error after 2-point calibration

FPGA Smart Temperature Sensor

- First FPGA thermal sensor
- Pure cell-based design
- Only 140 LEs used
- INL Error: -1.5~0.8°C for 0~75°C range
- Power: 8.4μW
- 70-LE version under measurement



Prototype & Result



Effective measurement errors of 10 FPGA chips with two- temperature calibration

P. Chen, TCAS-I 2007